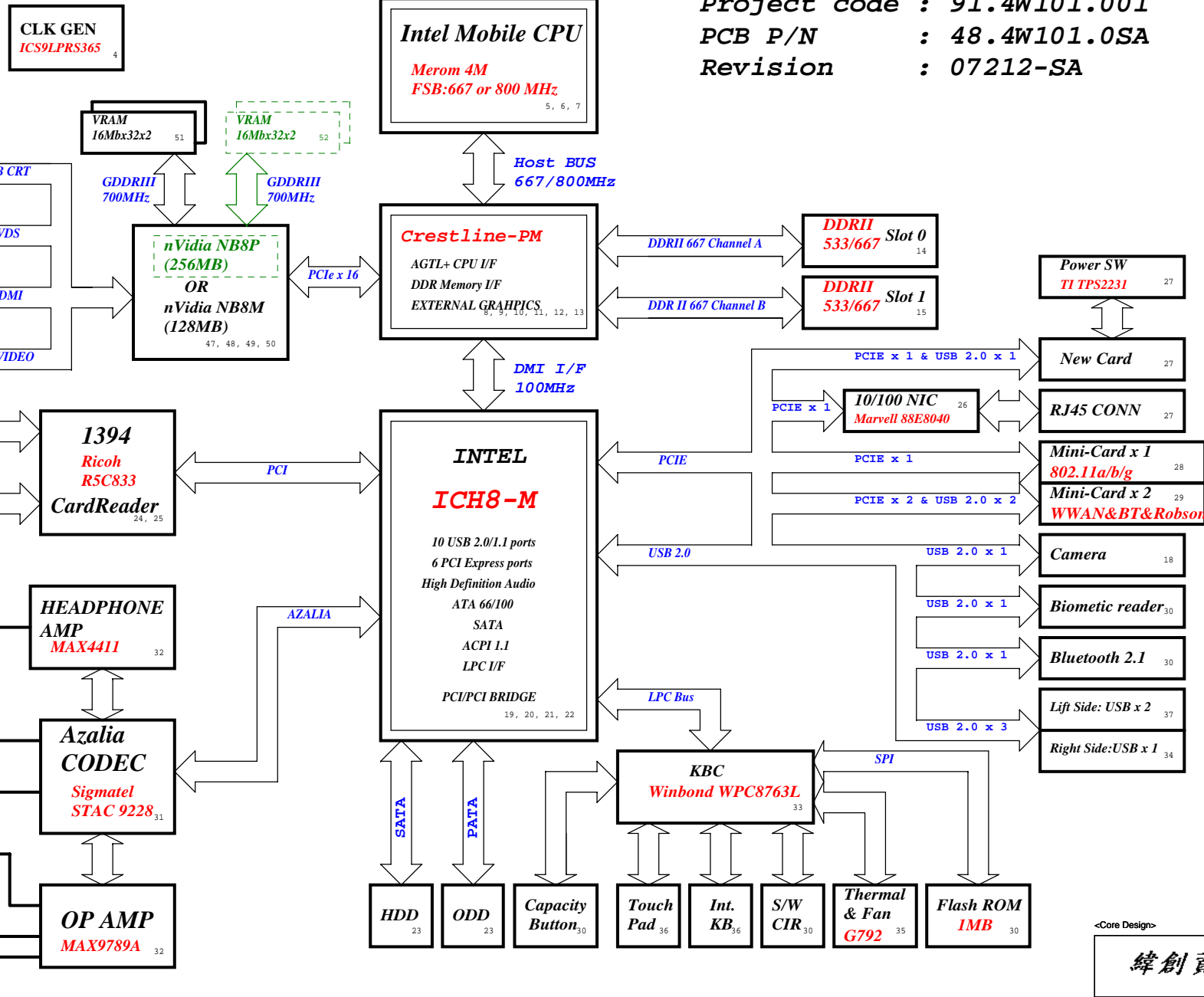


Hawke Intel Discrete Block Diagram

Project code : 91.4W101.001
PCB P/N : 48.4W101.0SA
Revision : 07212-SA



BATTERY CHARGER MAX8731A		38
INPUTS	OUTPUTS	
AD+ BAT+	DCBATOUT	
SYSTEM DC/DC TPS51120		39
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	
SYSTEM DC/DC TPS5117		42, 43
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0 1D8V_S3	
SYSTEM DC/DC TPS51100		44
INPUTS	OUTPUTS	
1D8V_S3	0D9V_S3	
SYSTEM DC/DC RT9018		44
INPUTS	OUTPUTS	
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0	
VGA DC/DC TPS5117		53
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFX_CORE_S0	
CPU DC/DC ISL6262A		40
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
PCB LAYER		
L1:TOP		
L2:GND		
L3:Signal		
L4:Signal		
L5:VCC		
L6:Singal		
L7:GND		
L8:BOT		

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

System Block Diagram		
Size	Document Number	Rev
A3	Hawke-Intel	SA
Date:	Tuesday, May 08, 2007	Sheet 1 of 55

Adapter

AD_OFF	Input Signal (I)	Output Signal (O)	AD_IN
AD_JK	Input Power	Output Power	AD+
5V_AUX_S5	VCC(I)	VCC(O)	
	VCC(I)		

TPS51117 1D8V

PM_SLP_S4#	Input Signal EN_PSV(I / 5V)	Output Signal (O)	CPUCORE_ON
5V_S5	Input Power	Output Power	
DCBATOUT	VIN	(O)	1D8V_S3(19A)

TPS51117 1D05V

PM_SLP_S3#	Input Signal EN_PSV(I / 5V)	Output Signal (O)	CPUCORE_ON
5V_S5	Input Power	Output Power	
DCBATOUT	VIN	(O)	1D05V_S0(5A)

Charger_ISL6255

CHARGE_OFF	Input Signal CLS (I / 3.3V)	Output Signal LDO (O / 5.4V)	AD_IN
BT_TH	THM (I / 3.3V)	XTAL2/PB4 (O/5V)	CHARGE_LED#
BAT+SENSE	BATT (I / 3.3V)	XTAL1/PB3 (O/5V)	BL2#
BT_SCL_5	SCL (IO / 5V)		
BT_SDA_5	SDA (IO / 5V)		
FLASH_GPIO1	RESET#/PB5 (I/5V)	VCC (O)	DCBATOUT
FLASH_GPIO2	PB0/MOSI/AIN0	VCC (O)	BT+
AC_IN	PB0/MOSI/AIN0		
AD+	Input Power DCIN (I)		

TI TPS51100 0.9V/DDR_VREF_S3

PM_SLP_S4#	Input Signal S5		
PM_SLP_S4#	S3		
5V_S5	Input Power VCC(I)	Output Power VCC(O)	DDR_VREF_S3
1D8V_S3	VN(I)	VCC(O)	DDR_VREF_S0

RT9018A 1D5V

PM_SLP_S3#	Input Signal EN(I / 5V)	Output Signal (O)	CPUCORE_ON
5V_S5	Input Power VCC	Output Power	
1D8V_S3	VIN	(O)	1D5V_S0(2.2A)

ISL6262A CPU_CORE

CPU_VID0	VID Setting VID0(I / 3.3V)	Output Signal VROK()	VGATE_PWRGD
CPU_VID1	VID1(I / 3.3V)		
CPU_VID2	VID2(I / 3.3V)		
CPU_VID3	VID3(I / 3.3V)	Output Power	
CPU_VID4	VID4(I / 3.3V)		
CPU_VID5	VID5(I / 3.3V)		
CPU_VID6	VID6(I / 3.3V)	VCC_CORE_PWR(O)	VCC_CORE_S0 (Imax=47A)
CPUCORE_ON	Input Signal EN (I / 3.3V)		
VCC_SENSE	Voltage Sense VSEN(I / Vcore)		
VSS_SENSE	RGND(I / Vcore)		
DCBATOUT	Input Power VCC(I)		
5V_S0	VCC(I)		
3D3V_S0	VCC(I)		

TI TPS51120 3D3V/5V

3V/5V_EN	Input Signal 51120_EN2 FOR 3.3V	Output Signal PGOUT(OD / 5V)	CPUCORE_ON
3V/5V_EN	51120_EN1 FOR 5.0V		
DCBATOUT	Input Power VIN	Output Power 5V(O)	5V_AUX_S5
5V_AUX_S5	REG5V_IN(I / 5V)	3D3V(O)	3D3V_AUX_S5
			5V_S5 (6A)
			3D3V_S5 (5A)

RT9018A 1D25V

PM_SLP_S3#	Input Signal EN(I / 5V)	Output Signal (O)	CPUCORE_ON
5V_S5	Input Power VCC	Output Power	
1D8V_S3	VIN	(O)	1D25V_S0(2.7A)

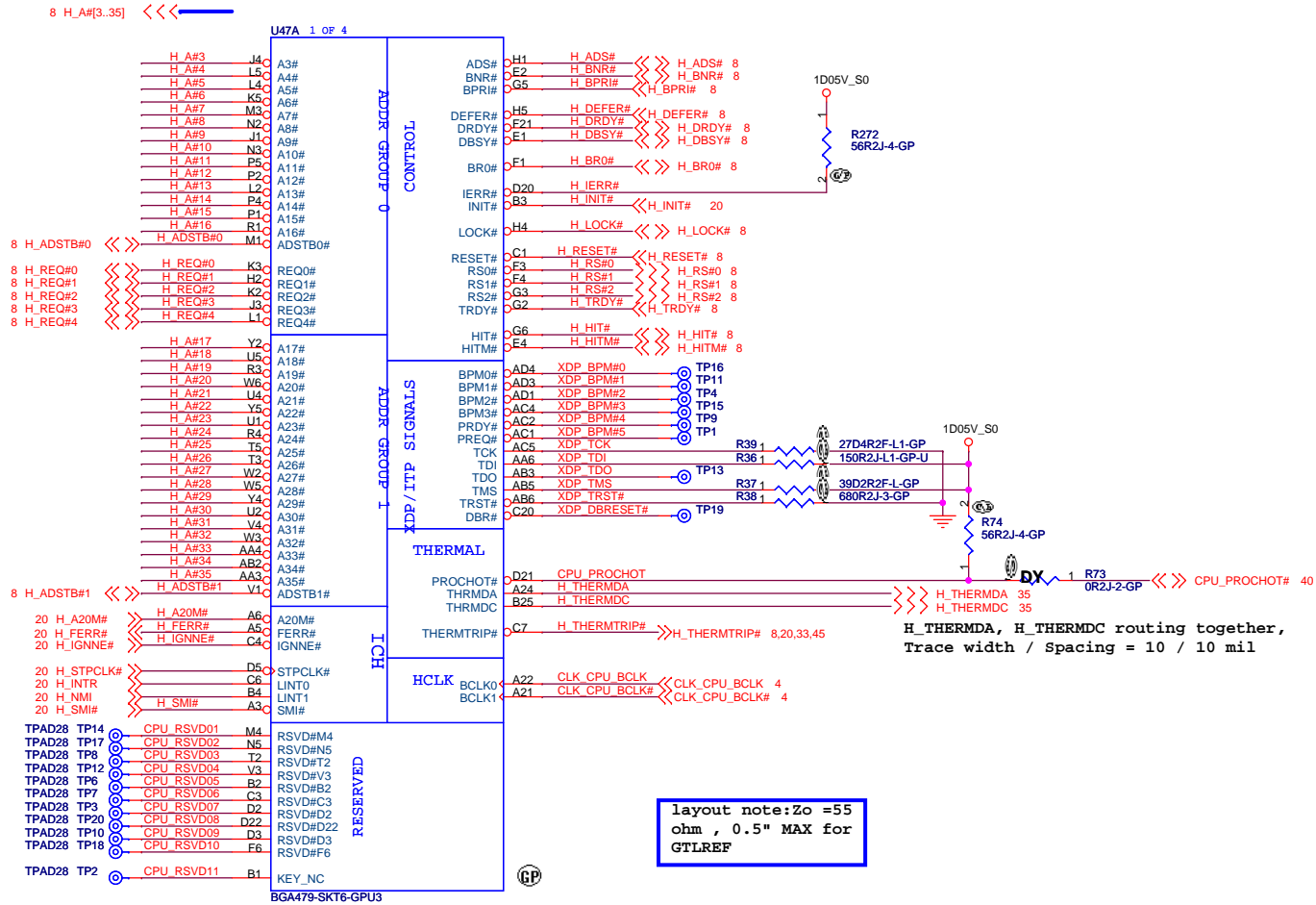
TPS51117 VGA_CORE

PM_SLP_S3#	Input Signal EN_PSV(I / 5V)	Output Signal (O)	CPUCORE_ON
5V_S5	Input Power VCC	Output Power	VCC_GFX_CORE_S0 (18.4A)
DCBATOUT	VIN	(O)	

<Core Design>

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Title	Power Block Diagram		
Size A3	Document Number	Rev SA	
Date: Tuesday, May 08, 2007	Sheet 2	of	55



Change to 62.10040.221 04/12 '07

<Core Design>

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Title		Meron(1/3)-AGTL+/XDP	
Size	Document Number	Hawke-Intel	
A3		SA	
Date:	Tuesday, May 08, 2007	Sheet	5 of 55

8 H_D#0[0.63] <<>>

8 H_DSTBN#0
8 H_DSTBP#0
8 H_DINV#0

8 H_DSTBN#1
8 H_DSTBP#1
8 H_DINV#1

4.8 CPU_BSEL0
4.8 CPU_BSEL1
4.8 CPU_BSEL2

PLACE C617 close to the TEST4 PIN,
make sure TEST3,TEST4,TEST5 trace
routing is reference to GND and
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

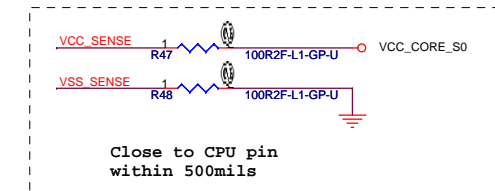
Resistor Placed
within 0.5" of CPU
pin. Trace should
be at least 25 mils
away from any other
toggling signal .
COMP[0,2] trace
width is 18 mils.
COMP[1,3] trace
width is 4 mils .

VCC_CORE_S0

VCC_CORE_S0

layout note:
place C618 near
PIN B26

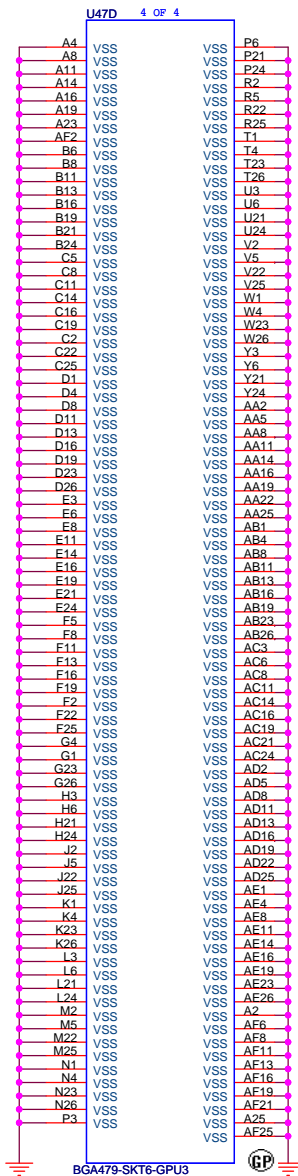
Length match within
25 mils . The trace
width/space/other is
20/7/25 .



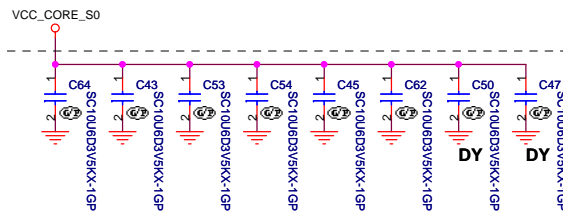
<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

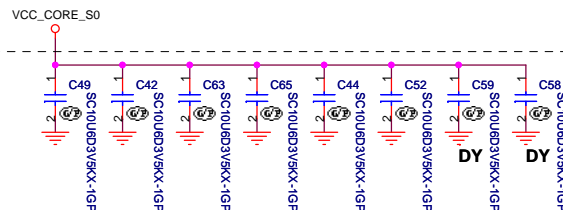
Title		
Meron(2/3)-AGTL+-PWR		
Size	Document Number	Rev
A3	Hawke-Intel	SA
Date:	Tuesday, May 08, 2007	Sheet 6 of 55



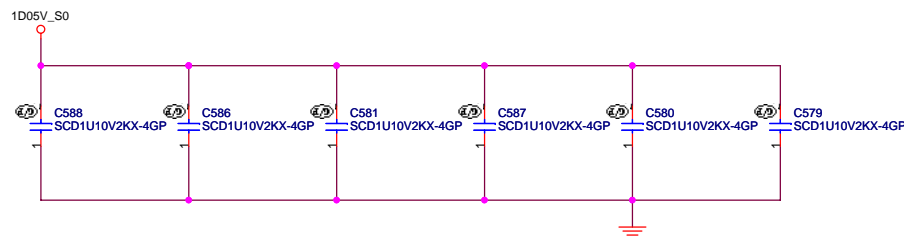
Place these capacitors on L1
(North side ,Secondary Layer)



Place these capacitors on L1
(North side ,Secondary Layer)



Mid Frequencd
Decoupling

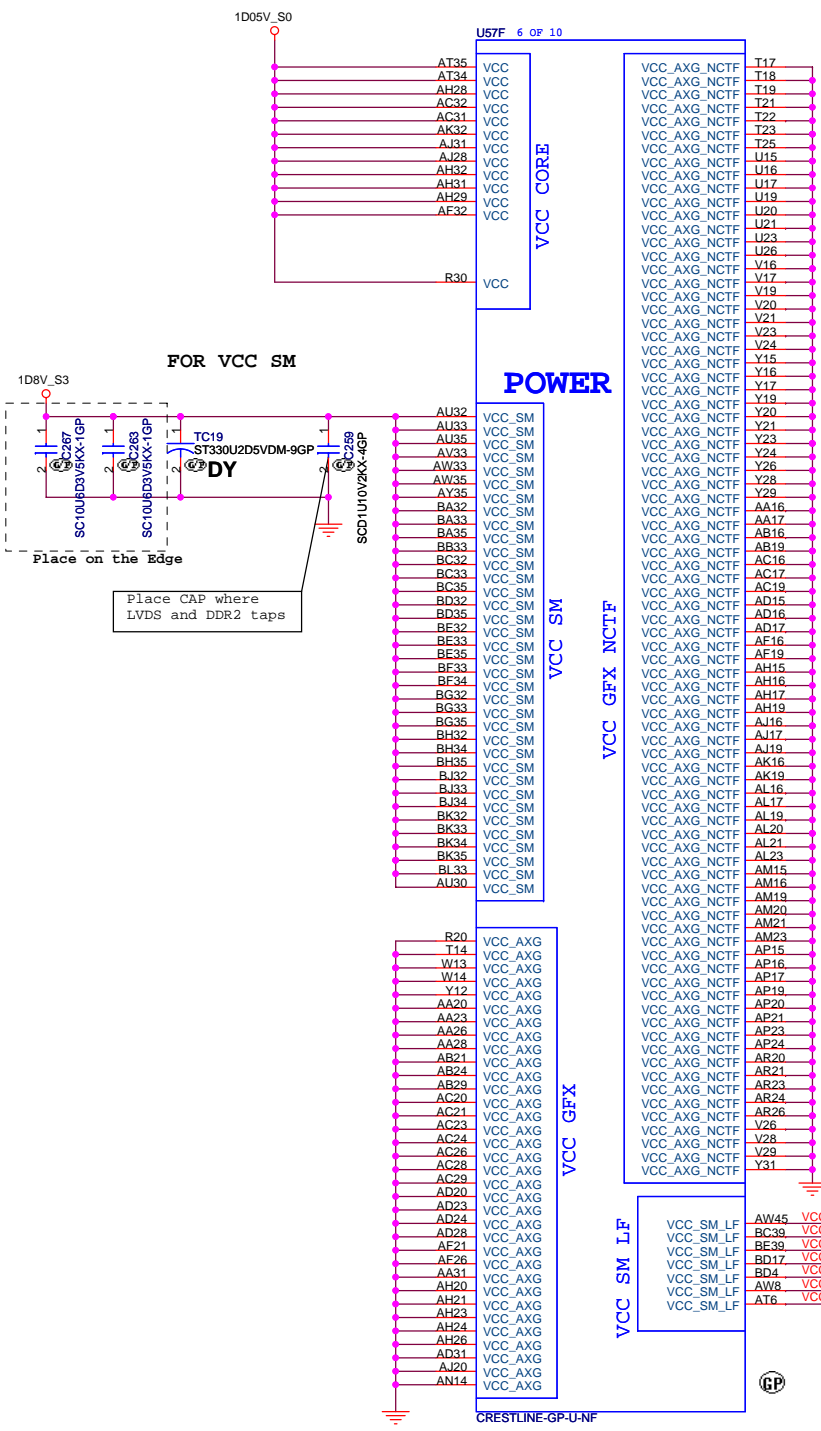


Place these
inside socket
cavity on L1
(North side
Secondary)

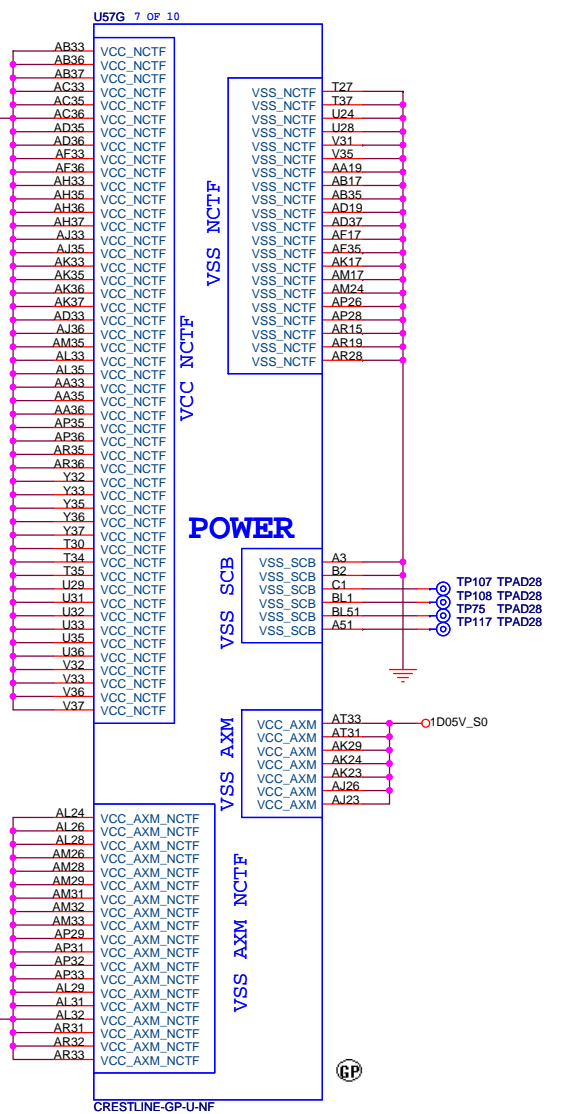
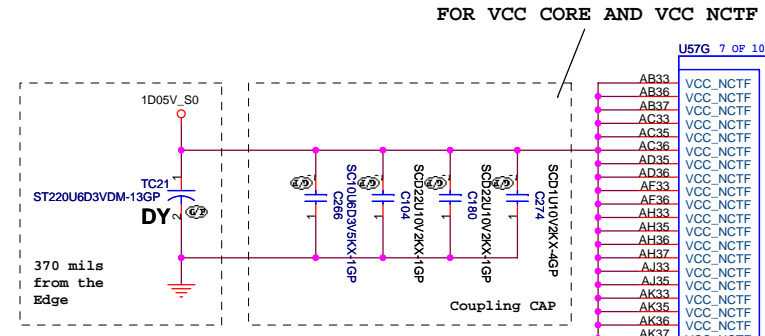
<Core Design>

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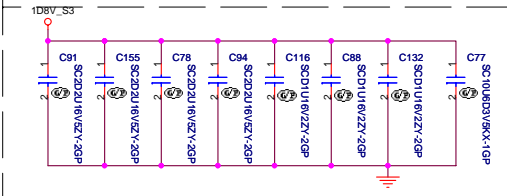
Title		Rev
Meron(3/3)-GND&Bypass		SA
Size A3	Document Number	
Date: Tuesday, May 08, 2007	Sheet 7 of 55	



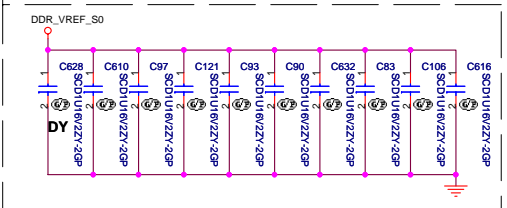
Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VTT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A
+1.25V_RUN	VCCA_AXF	0.35A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TV DAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A



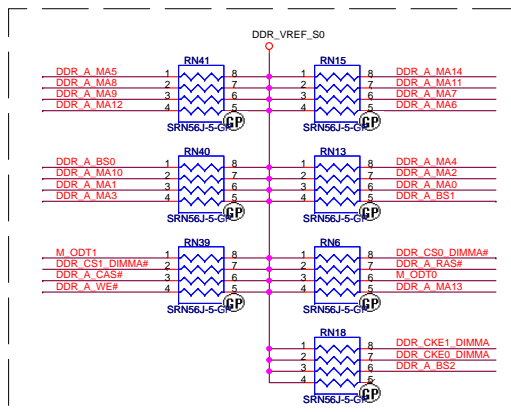
Layout Note:
Place near DM1



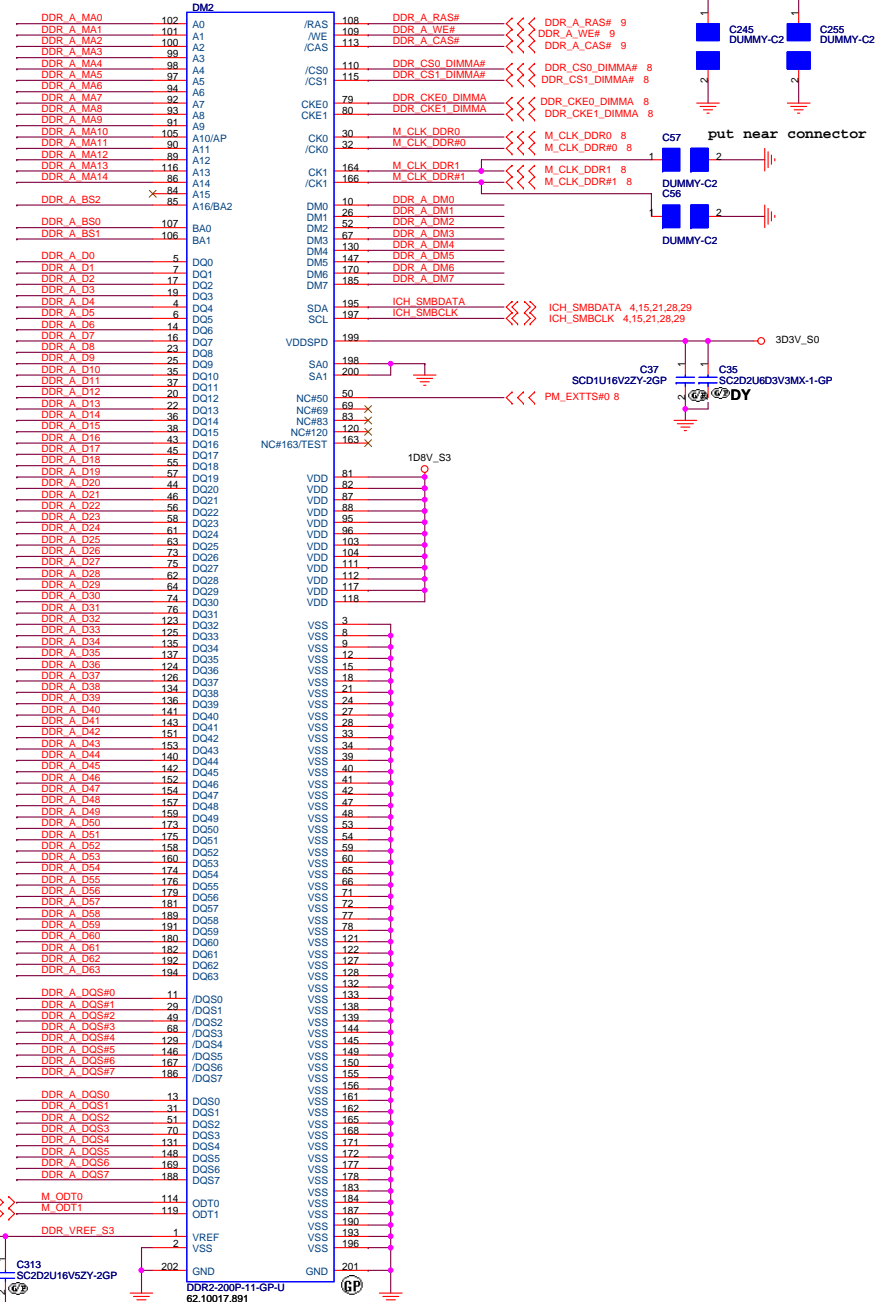
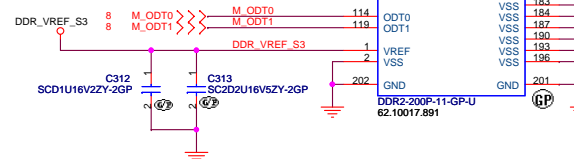
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



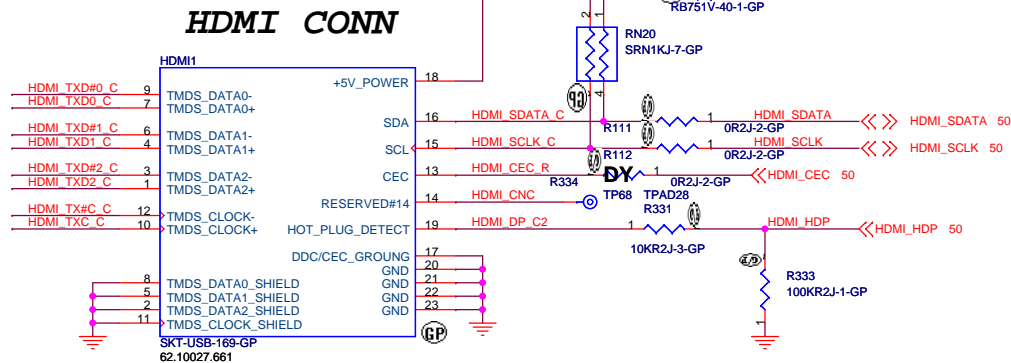
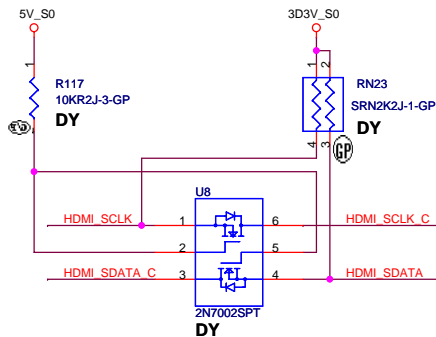
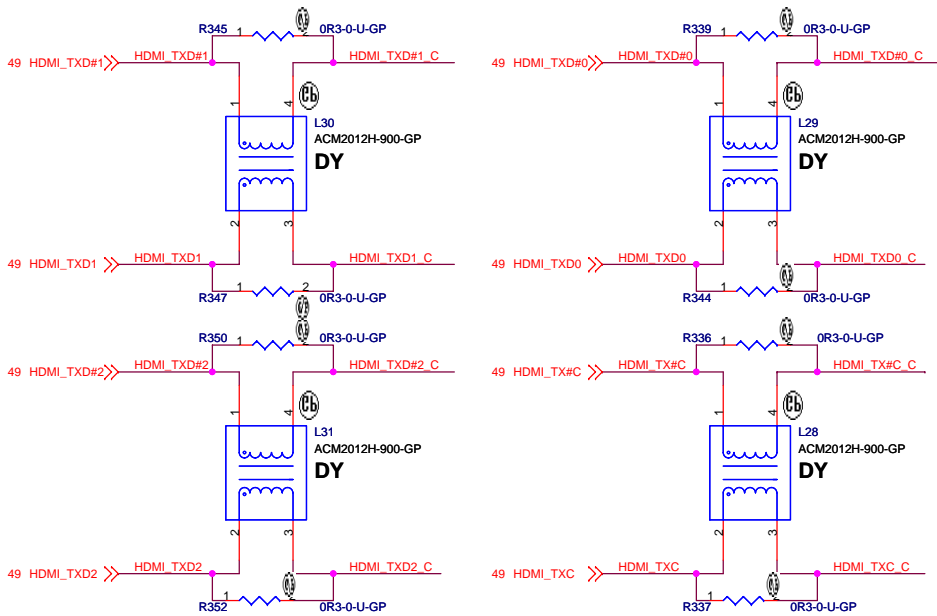
change to 8P4R



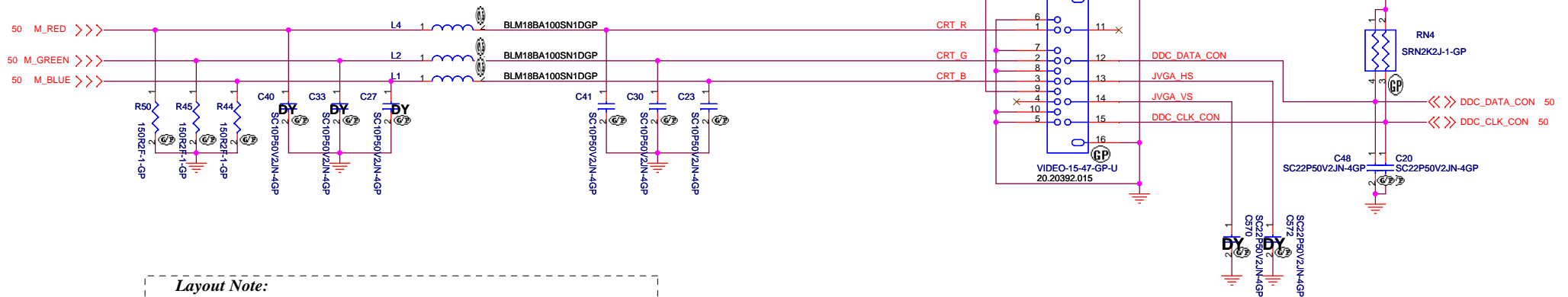
Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"



HDMI I/F & CONNECTOR

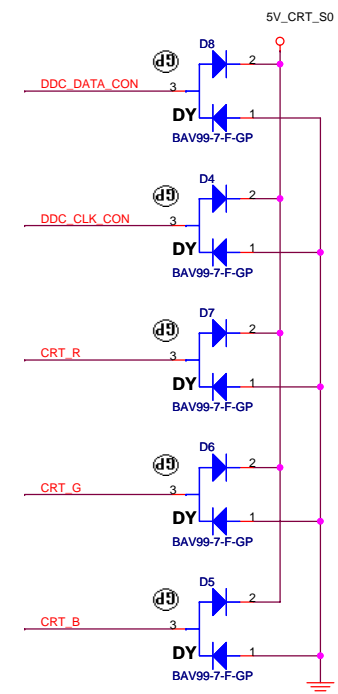
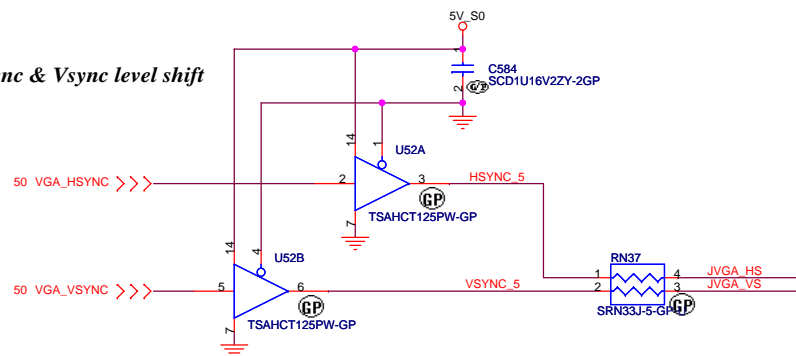


CRT I/F & CONNECTOR



Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

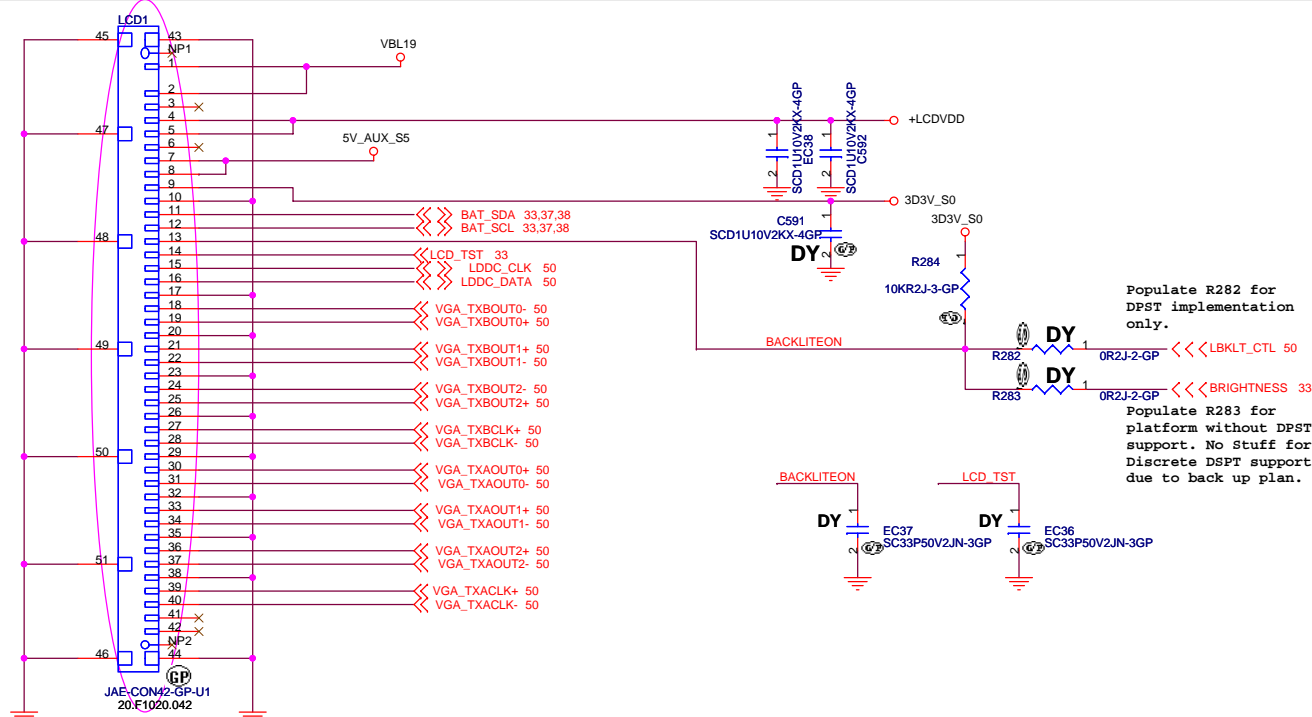
Hsync & Vsync level shift



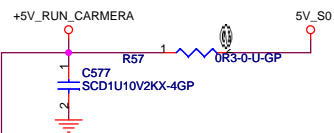
<Core Design>

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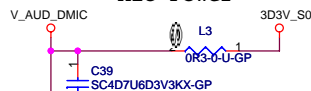
Title		CRT Connector	
Size A3	Document Number	Hawke-Intel	
Date: Tuesday, May 08, 2007	Sheet 17 of 55	Rev	SA



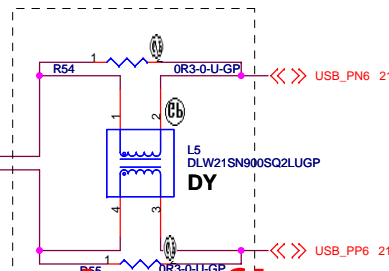
CAMERA Power



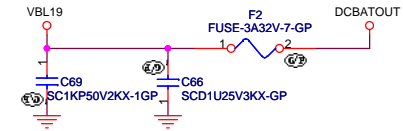
Mic Power



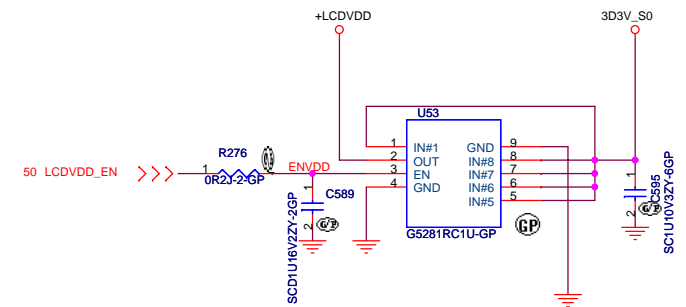
Place near connector CAMERA1.



INVERTER POWER



LCD POWER



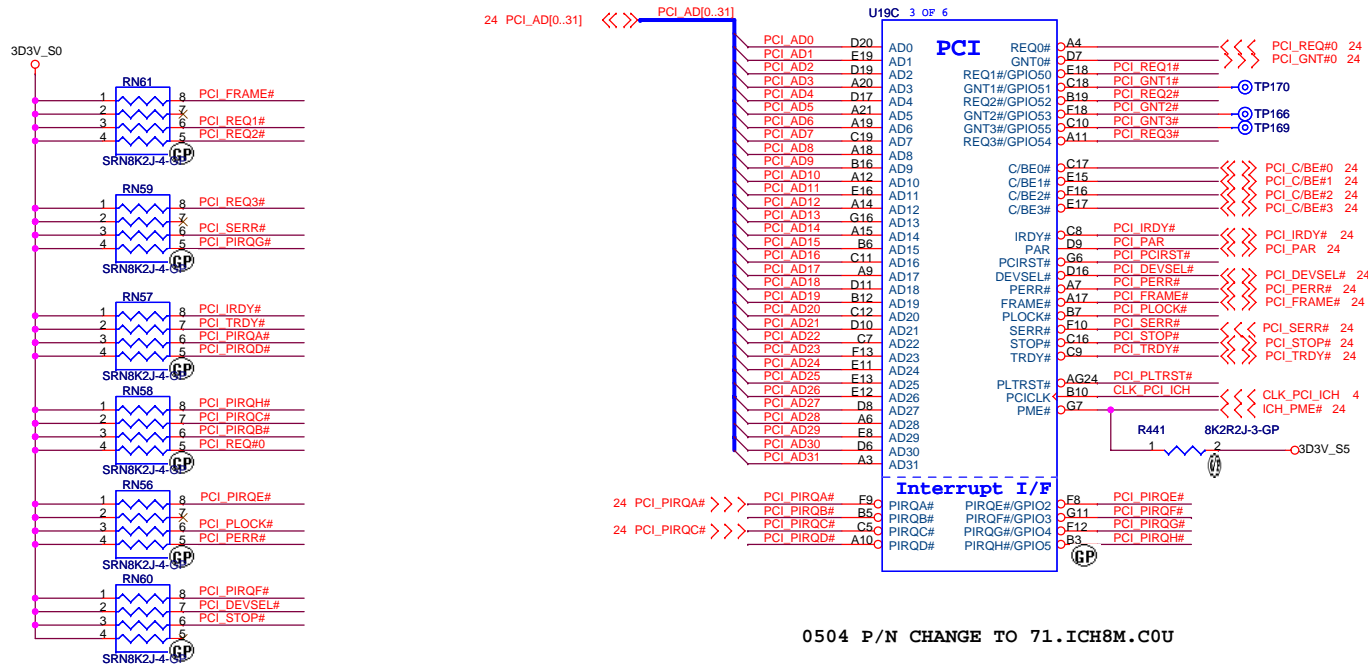
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		LCD/Inverter/Camera	
Size	Document Number	Rev	
A3		SA	
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PCI Interface Routing

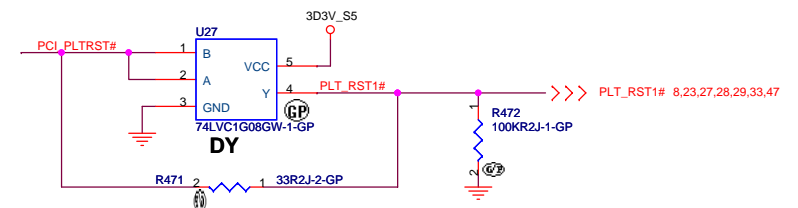
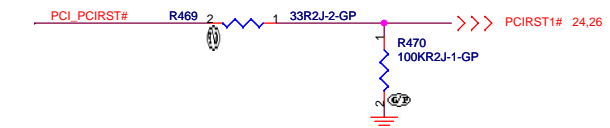
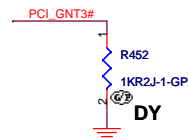
	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0



ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

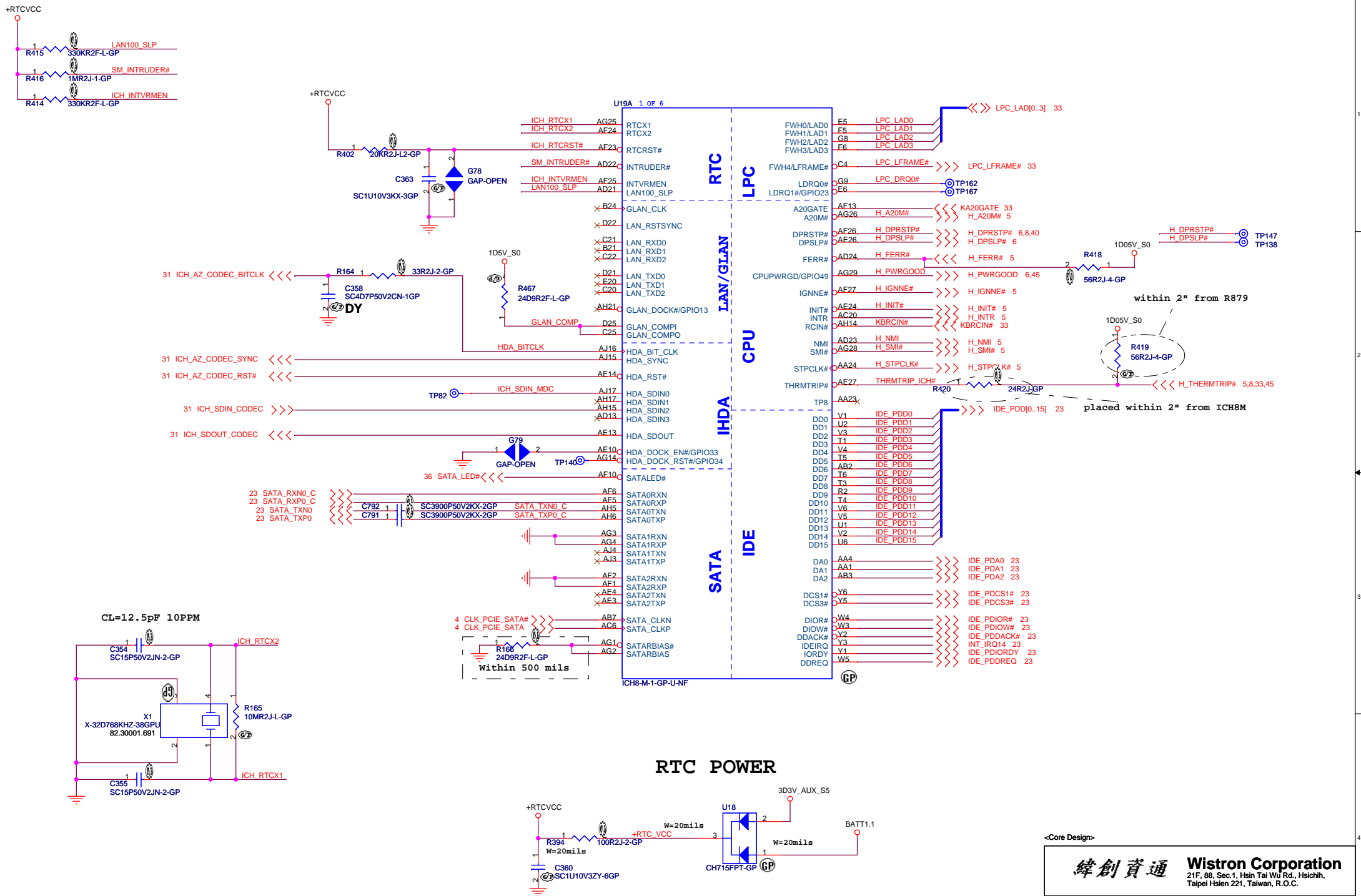
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



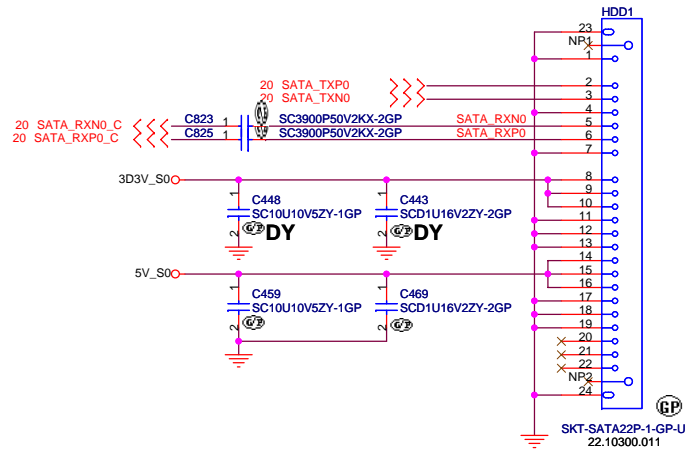
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

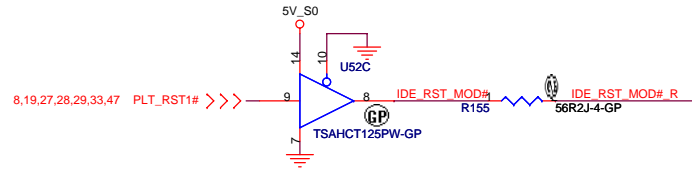
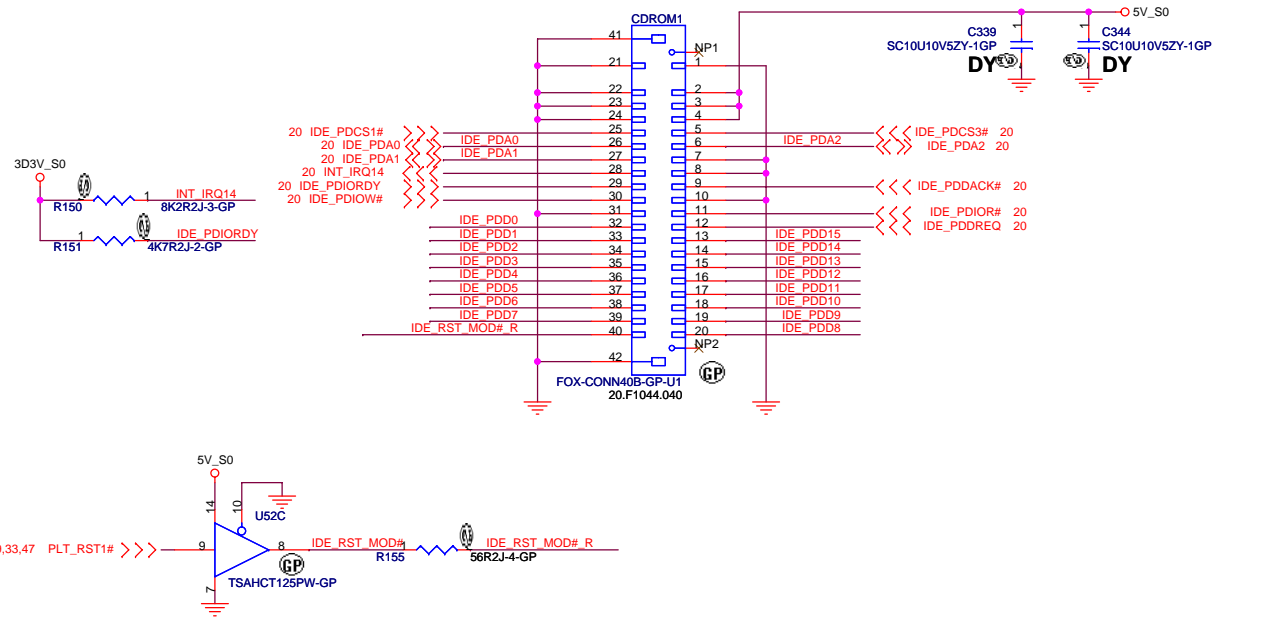
Title	ICH8(1/4)-PCI/INT		
Size A3	Document Number	Hawke-Intel	Rev SA
Date: Tuesday, May 08, 2007	Sheet 19	of 55	



SATA HDD Connector



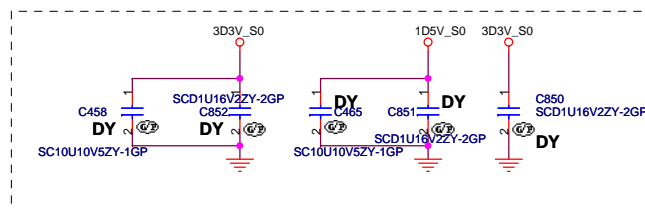
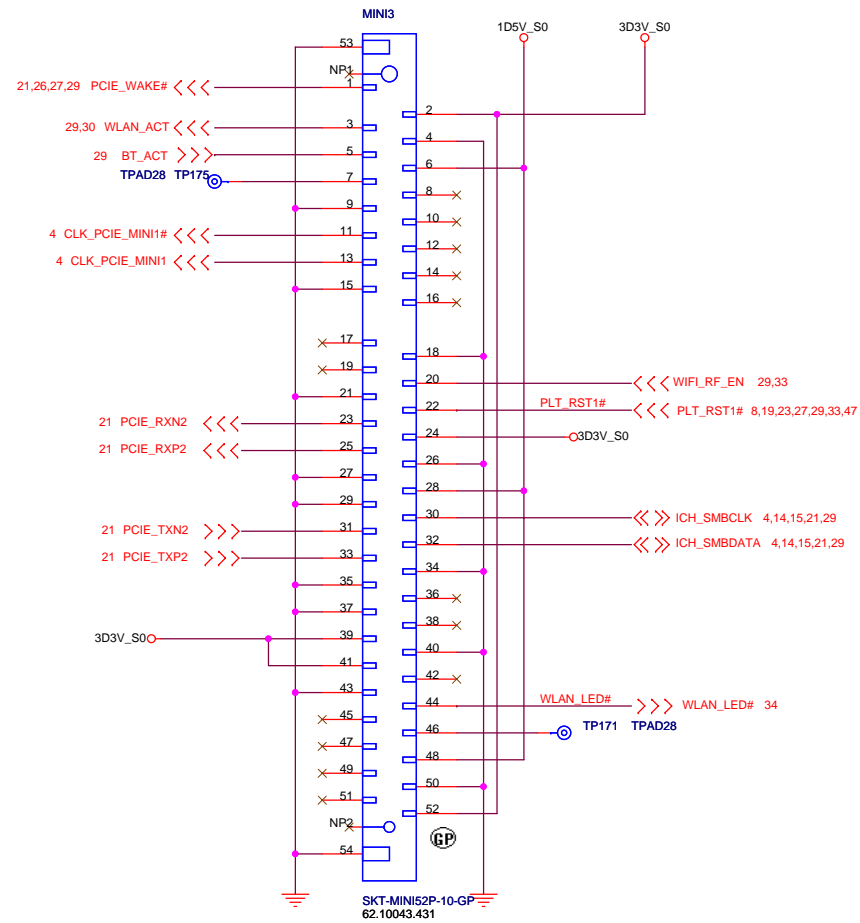
ODD Connector



<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		HDD/ODD	
Size A3	Document Number	Hawke-Intel	Rev SA
Date: Tuesday, May 08, 2007	Sheet 23	of	55

Mini Card Connector 2(802.11a/b/g)

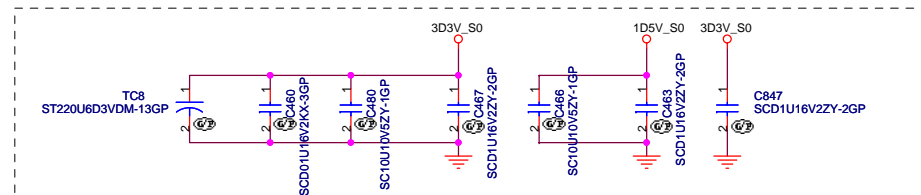
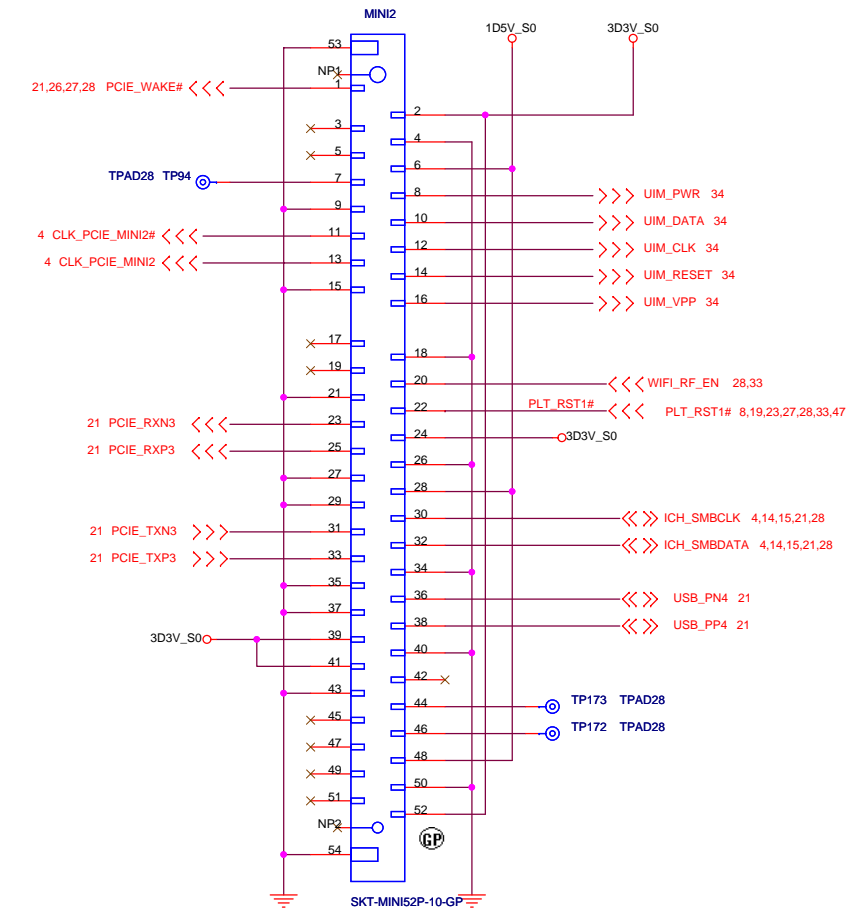


<Core Design>

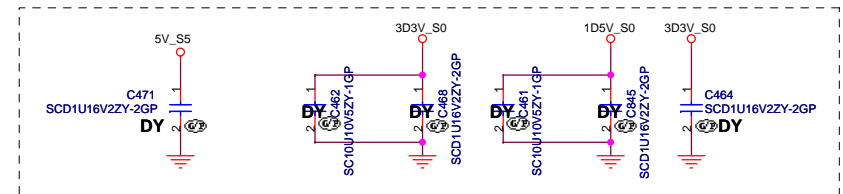
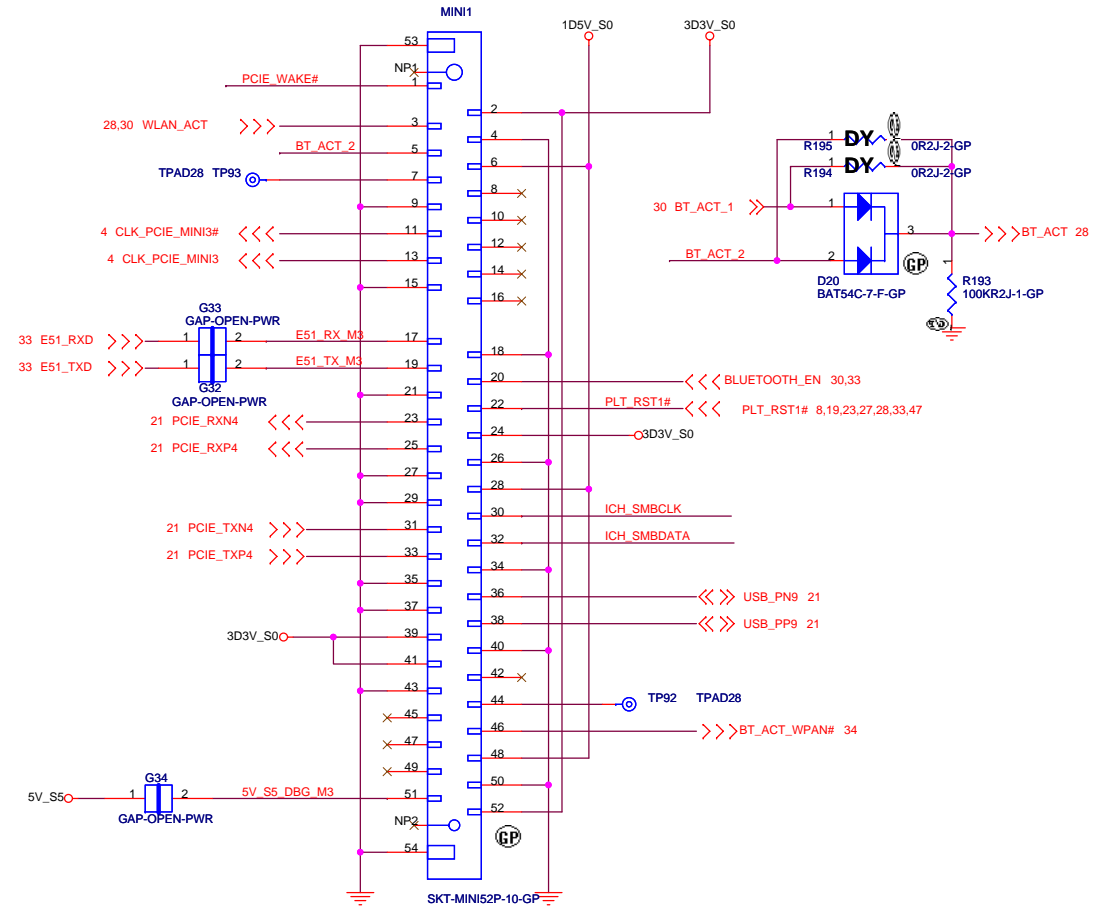
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI CARD CONN 1	
Title Size A3	Document Number Hawke-Intel
Date: Tuesday, May 08, 2007	Rev SA
Sheet 28 of 55	

Mini Card Connector

Mini Card Connector 2(WWAN)



Mini Card Connector 3(Robson/BT)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title				
MINI CARD CONN 2 & 3				
Size	Document Number			Rev
A3	Hawke-Intel			SA
Date:	Tuesday, May 08, 2007	Sheet	29 of	55

SPI FLASH ROM

SRN10KJ-6-GP
RN43

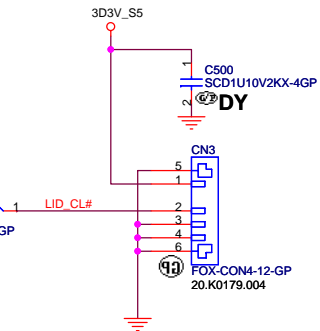
8M Bits

U61
W25X80-VSSI-GP

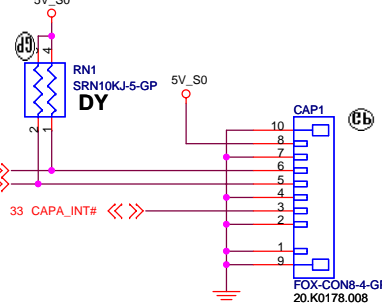
EMI REQUEST

Place close to EC

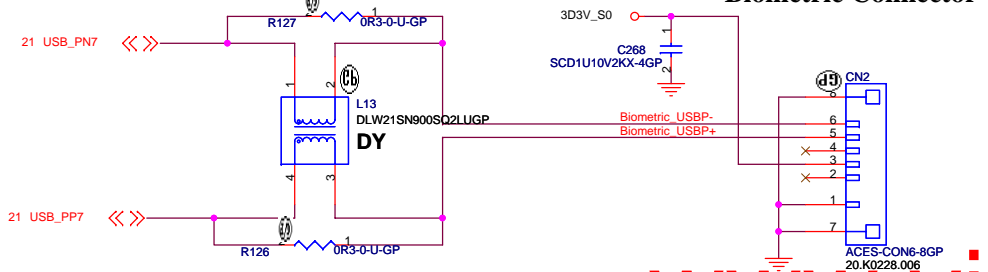
To Hall Switch



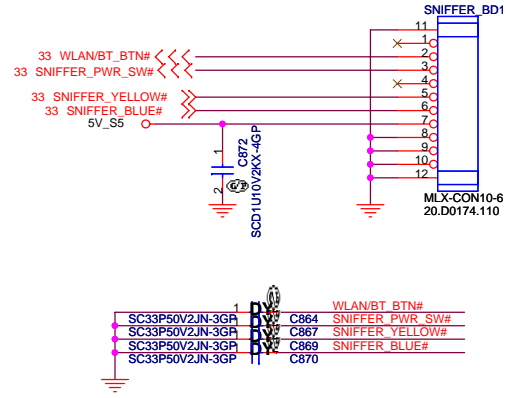
CAPACITY BUTTON



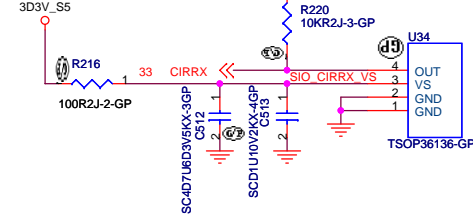
Biometric Connector



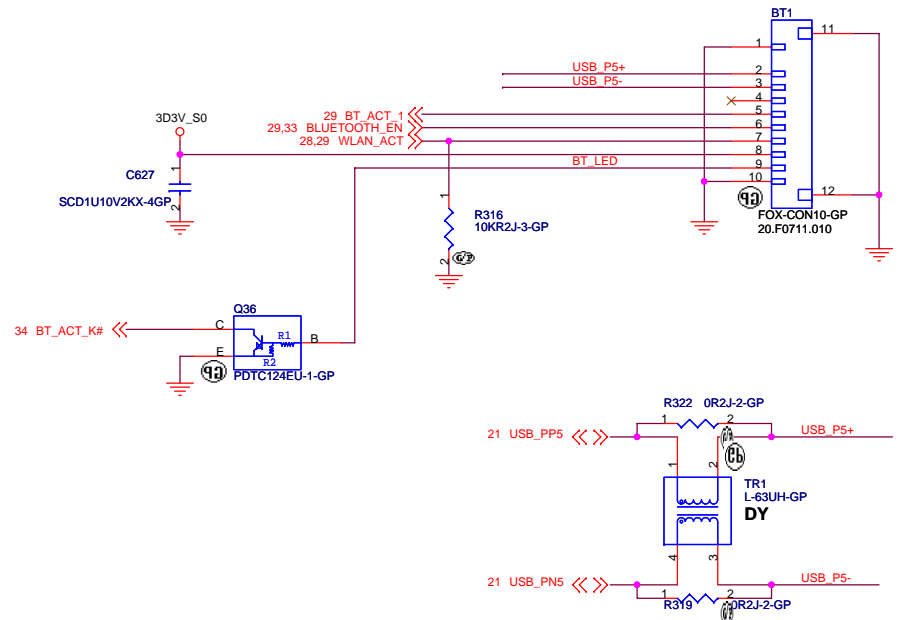
Switch Board



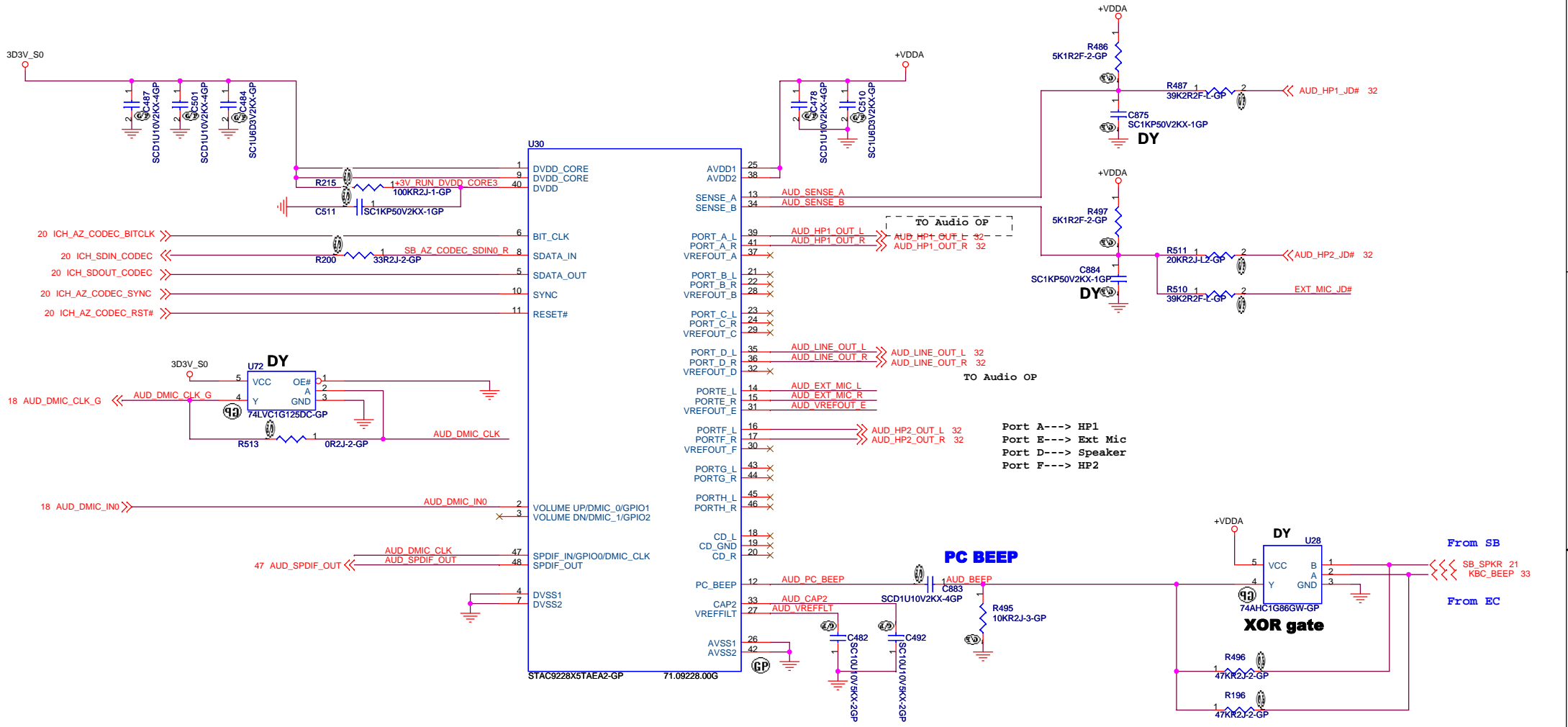
CIR



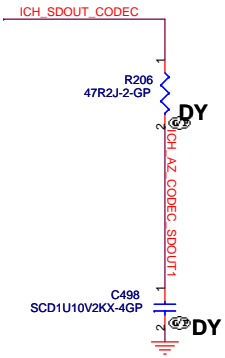
Bluetooth Module conn.



<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div>			
Title			
SBI/SNIFFER/CIR/BT/Biometric			
Size	Document Number	Rev	
A3		SA	
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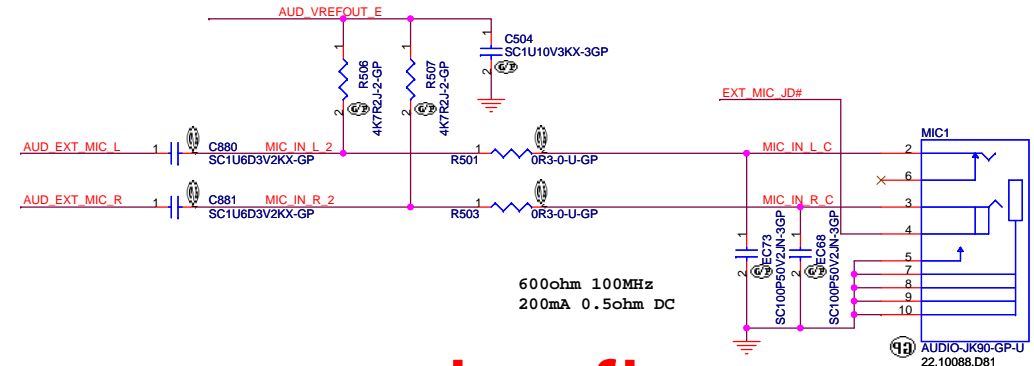
Azalia I/F EMI



Azalia I/F EMI



MIC IN



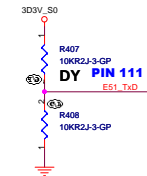
WPC8763L STRAP PIN

JENO (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	NO PD	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

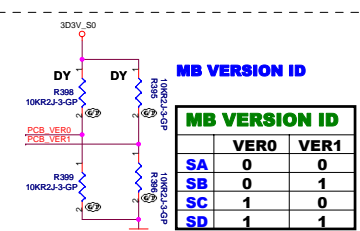
TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins, if an external 10 KΩ pull-down resistor is connected.

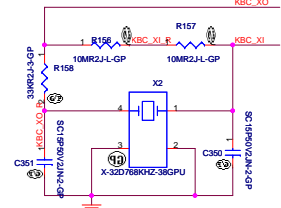
BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down resistor on BADDR1: Core defined



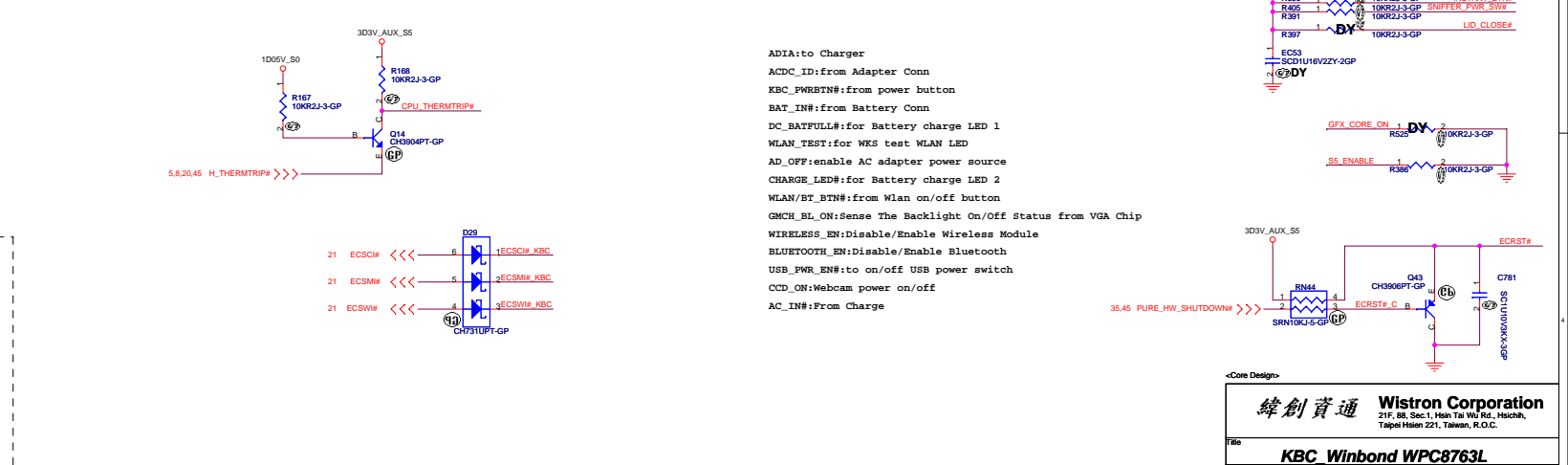
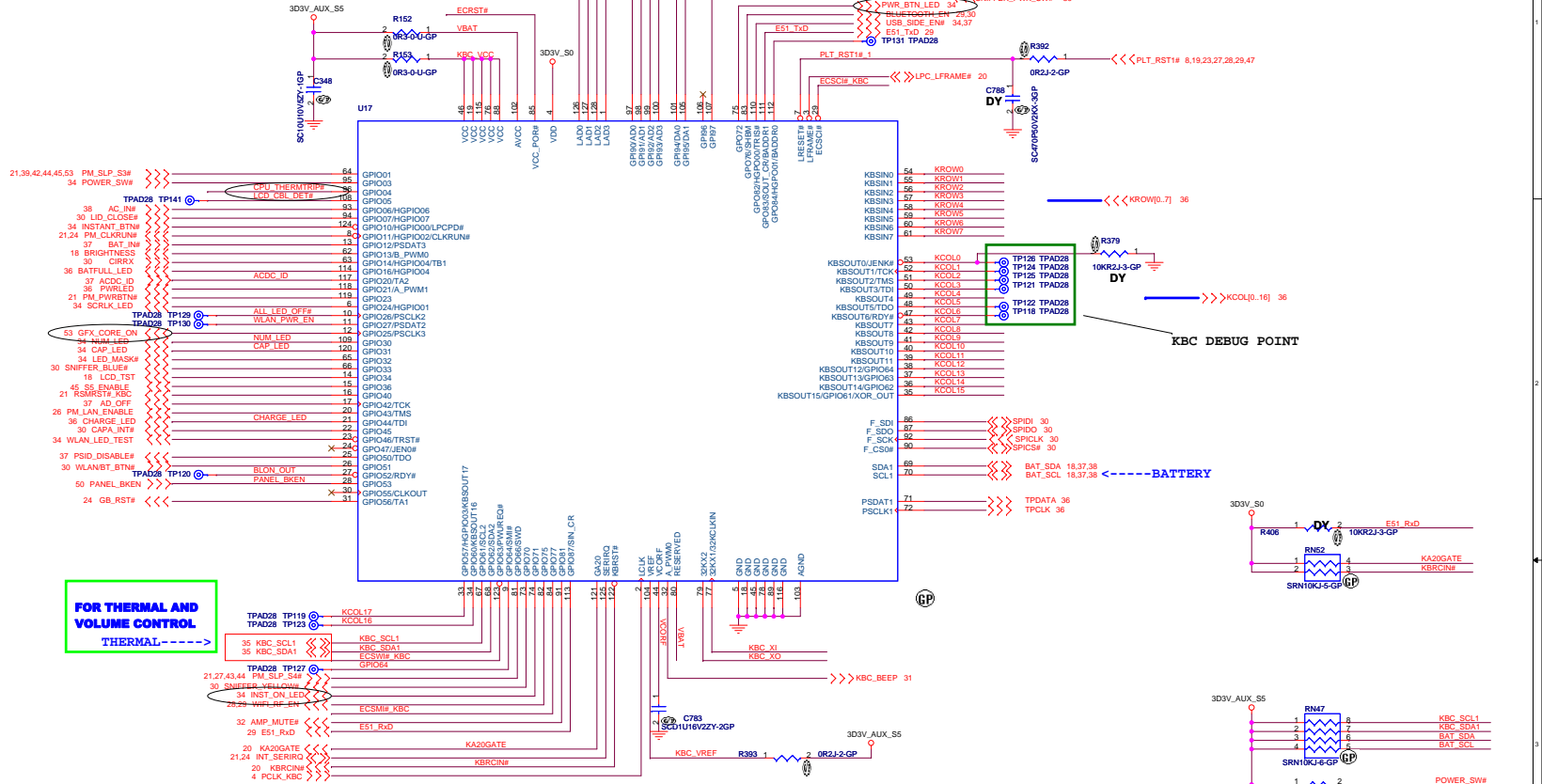
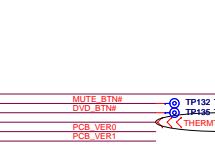
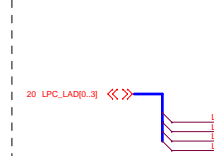
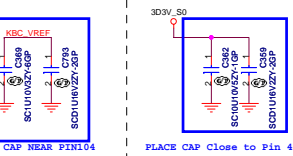
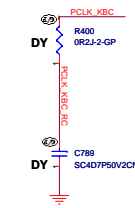
SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

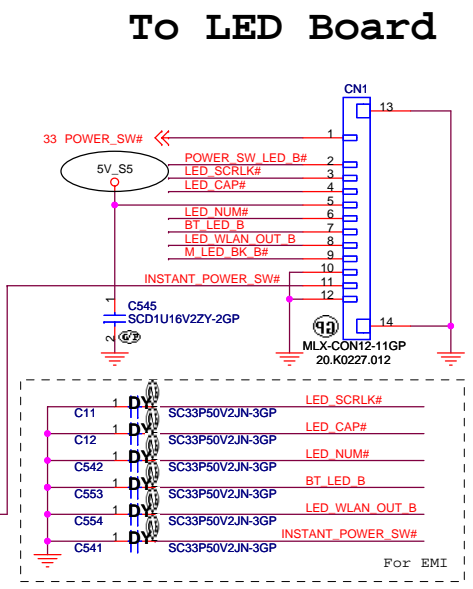
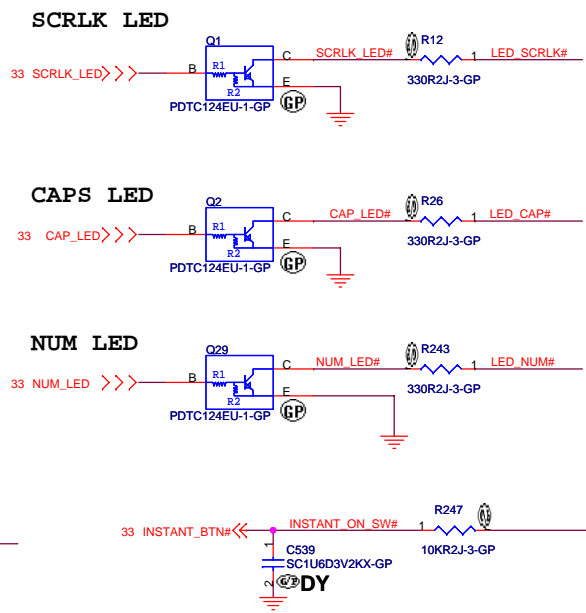
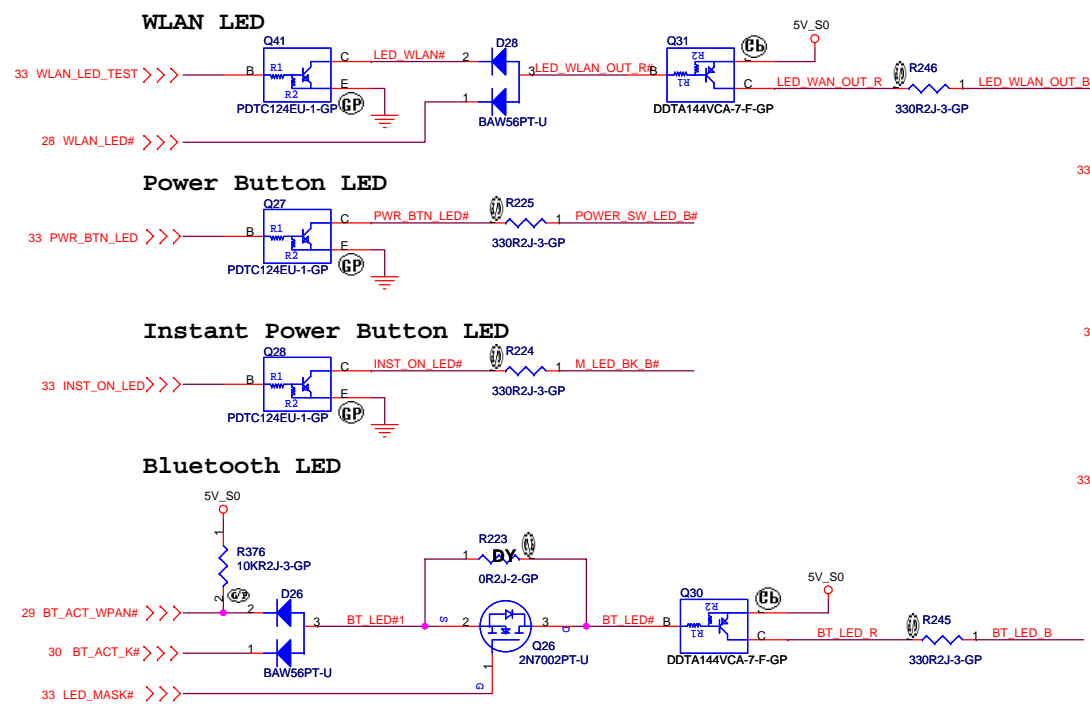


WPC8763L XTAL

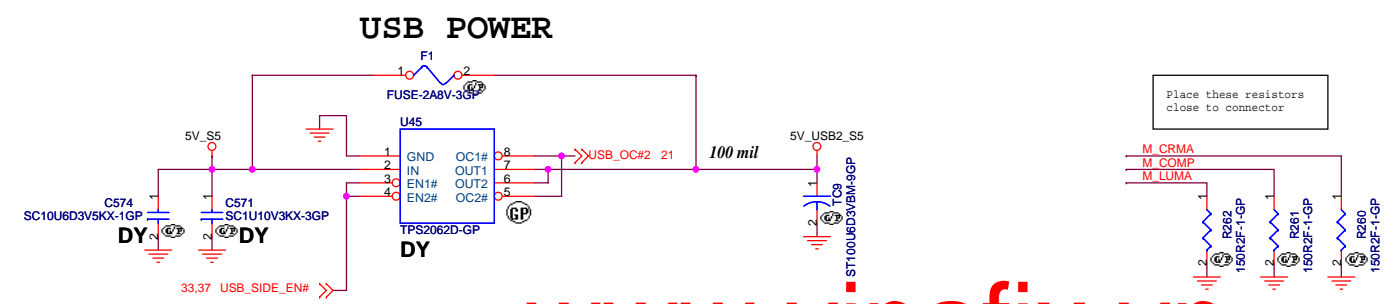
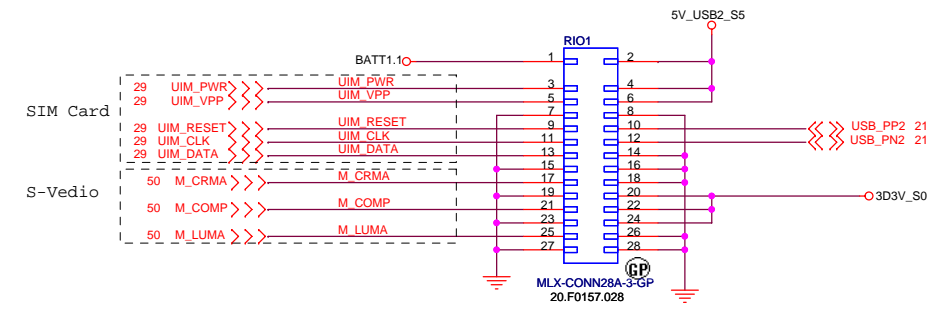


KBC CLK EMI





To Right I/O Board



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Right I/O/ Power Dash

SA

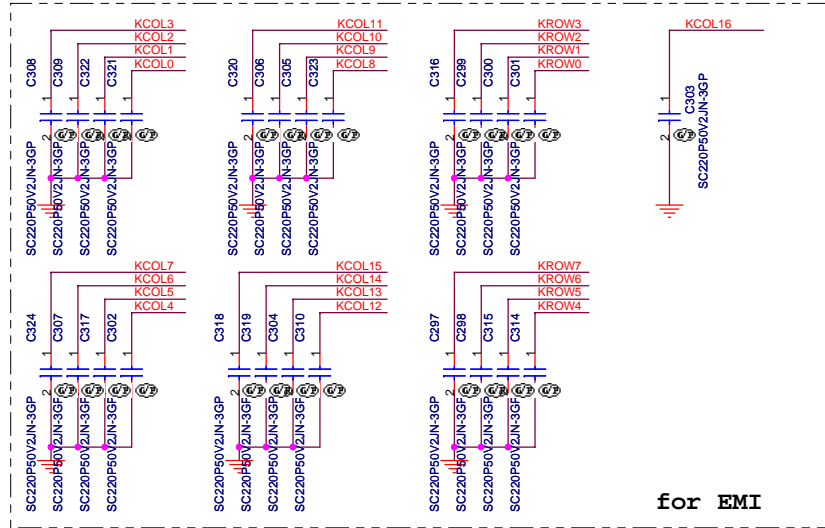
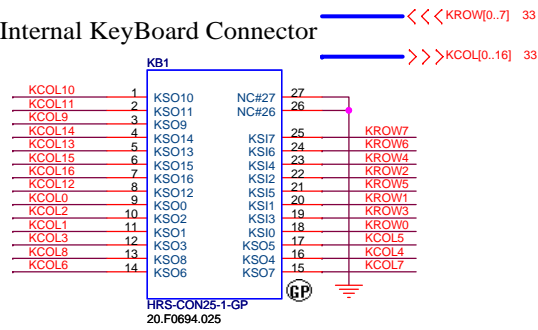
Size A3

Document Number

Date: Tuesday, May 08, 2007

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Internal KeyBoard Connector



LED NAME

ACTIVE SIGNAL

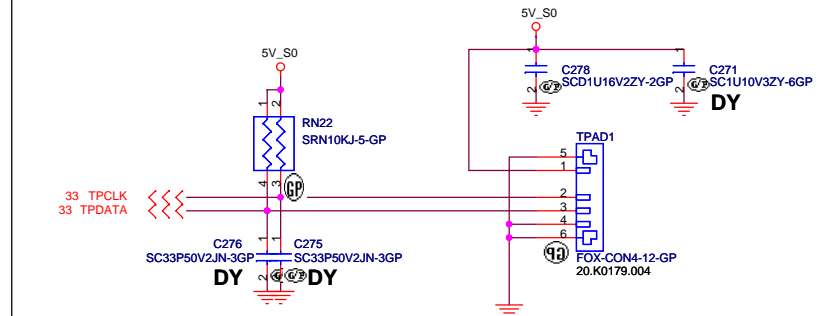
Power Button LED	PWR_BTN_LED
Instant Power Button LED	INST_ON_LED
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)
NUM LED	NUM_LED (from KBC)
SCRLK LED	SCRLK_LED (from KBC)
CAPS LED	CAP_LED (from KBC)

LED Board

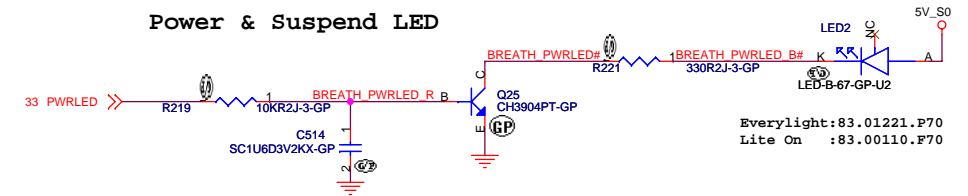
Main Board

Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC) CHARGE_LED

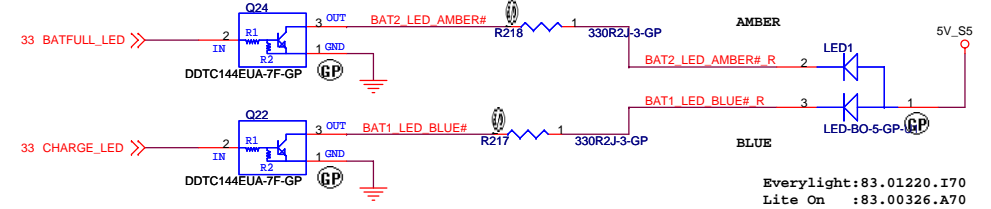
TouchPad Connector



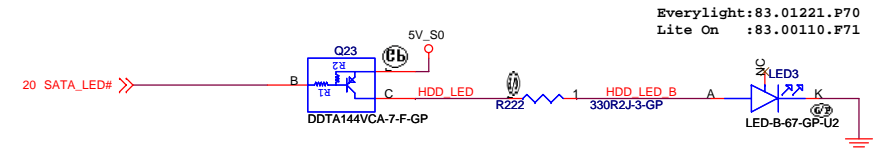
Power & Suspend LED



Battery LED



HDD LED

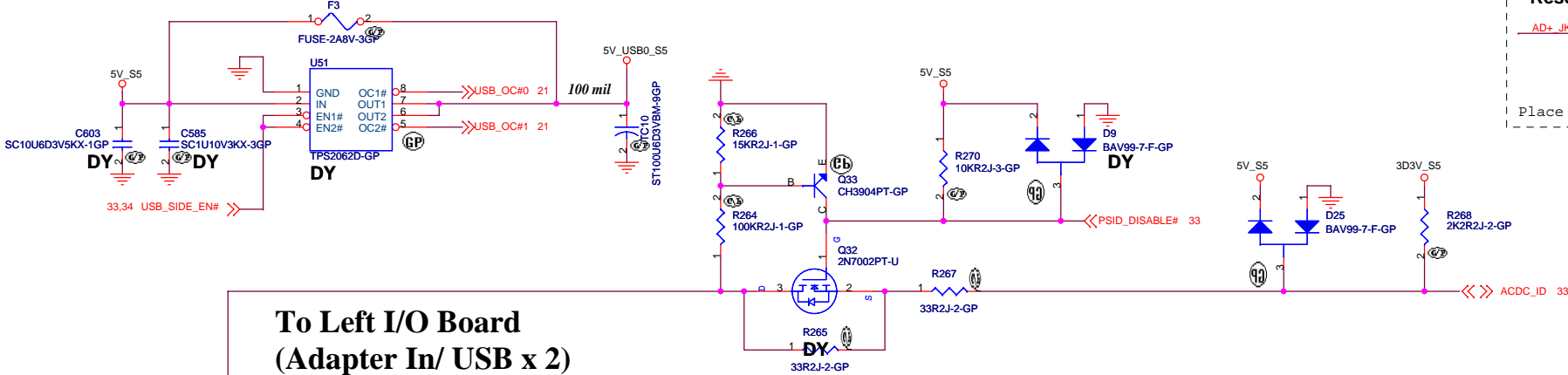


<Core Design>

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USB POWER



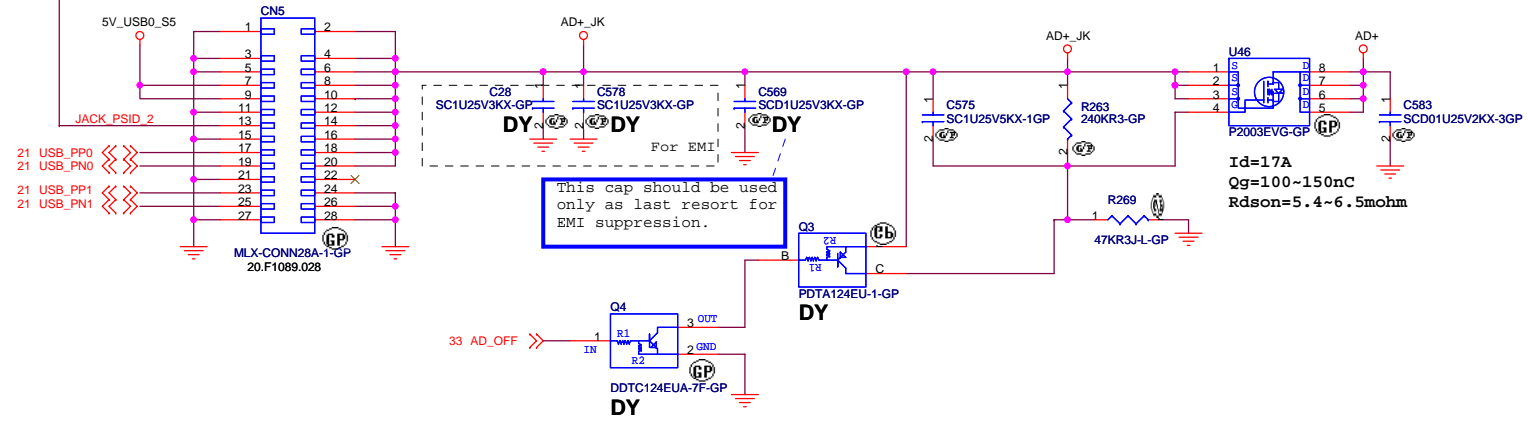
Reserved for EMI

AD+_JK

Place near CN13

C32 SCD01U25V2KX-3GP

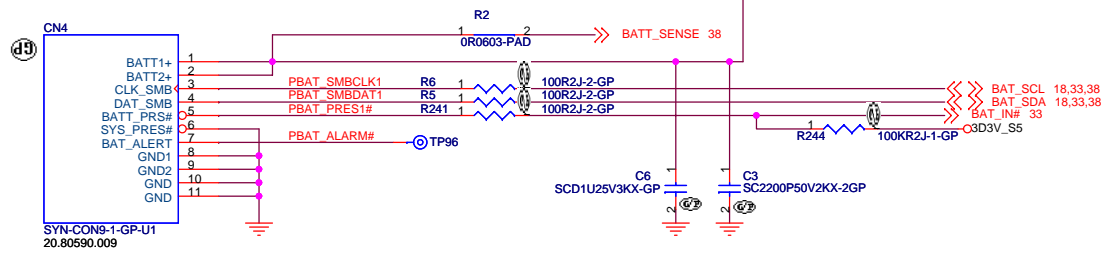
To Left I/O Board (Adapter In/ USB x 2)



This cap should be used only as last resort for EMI suppression.

Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm

Batt Connector



For EMI

PBAT_SMBCLK1 C5 1 SC33P50V2JN-3GP

PBAT_SMBDAT1 C4 1 SC33P50V2JN-3GP

PBAT_PREST1# C526 1 SC33P50V2JN-3GP

<Core Design>

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Title: **AD/BATT CONN**

Size: A3 Document Number: **Hawke-Intel** Rev: SA

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Place close to phase 1 choke

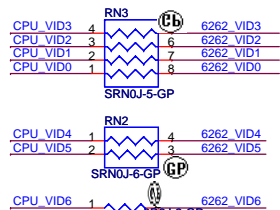
5 CPU_PROCHOT#



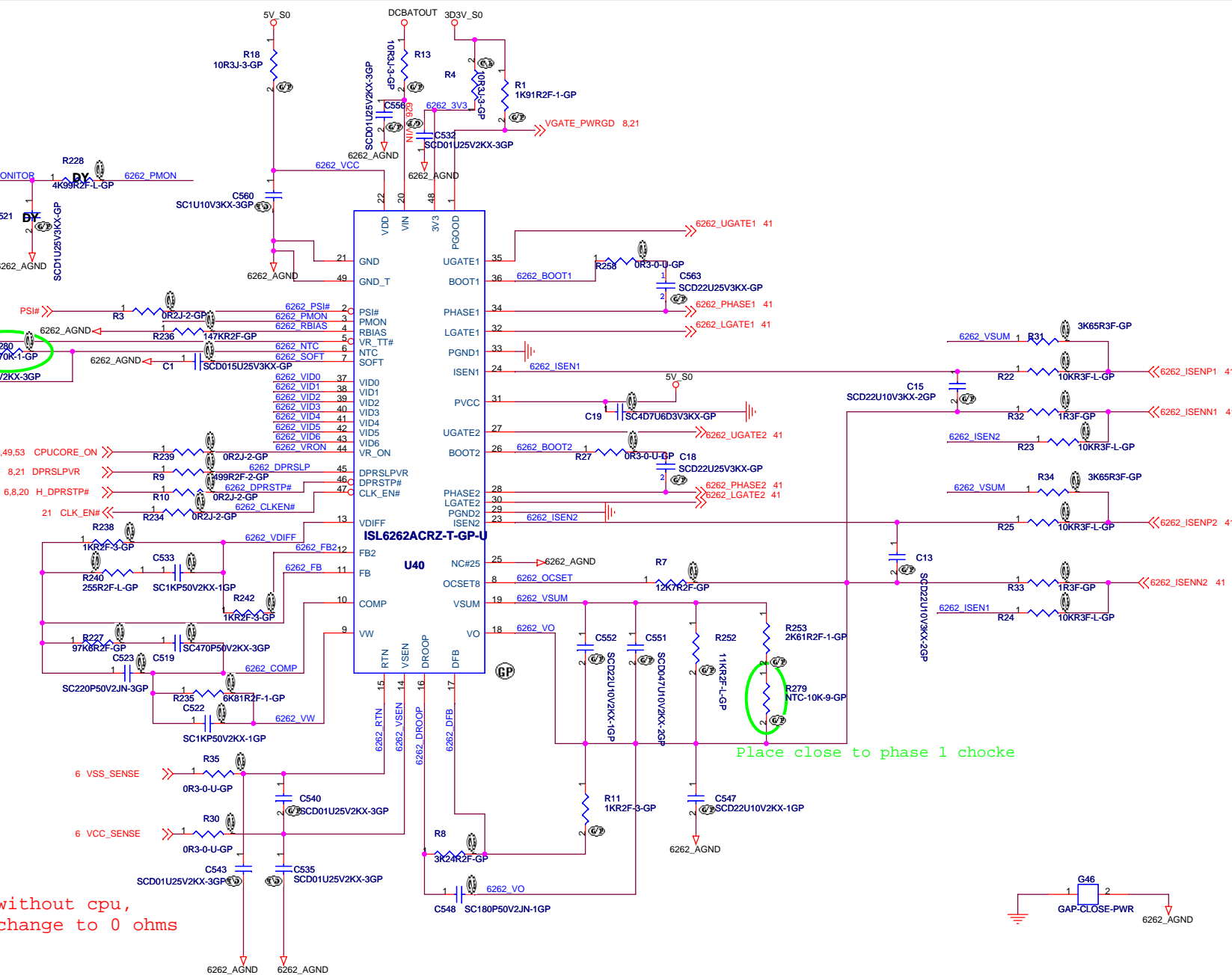
470K / 0402 size

If NTC=330Kohm, R285=8.66K

6 CPU_VID[0..6]



When test without cpu,
R30 & R35 change to 0 ohms

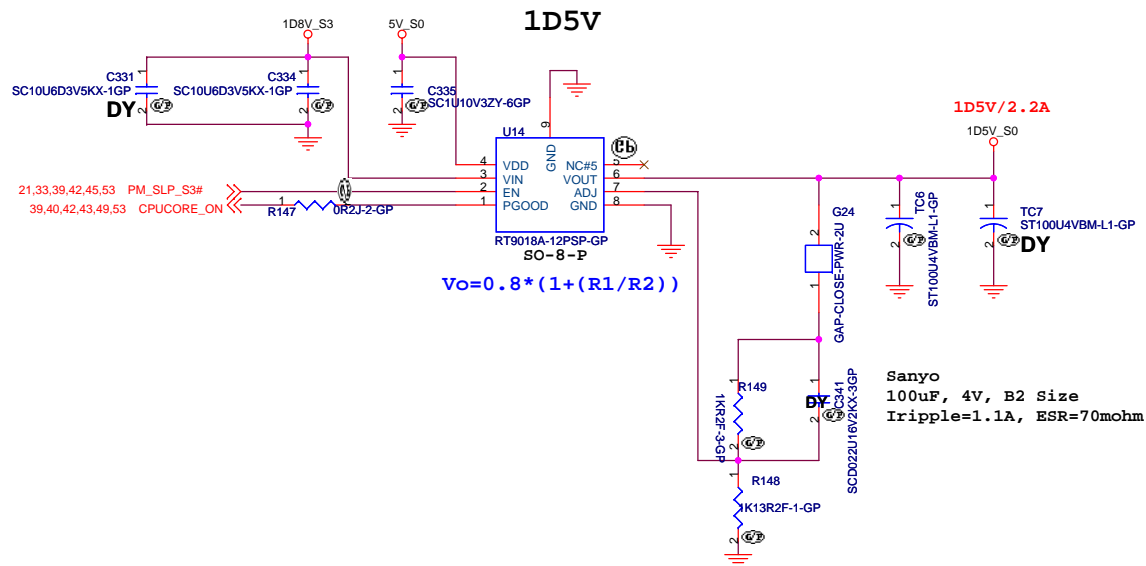


Place close to phase 1 choke

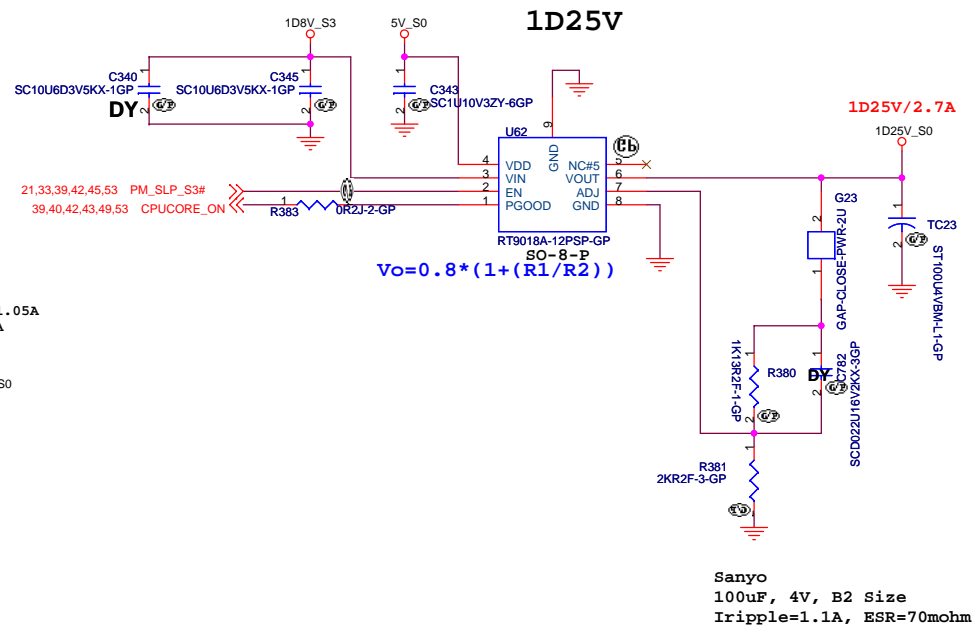
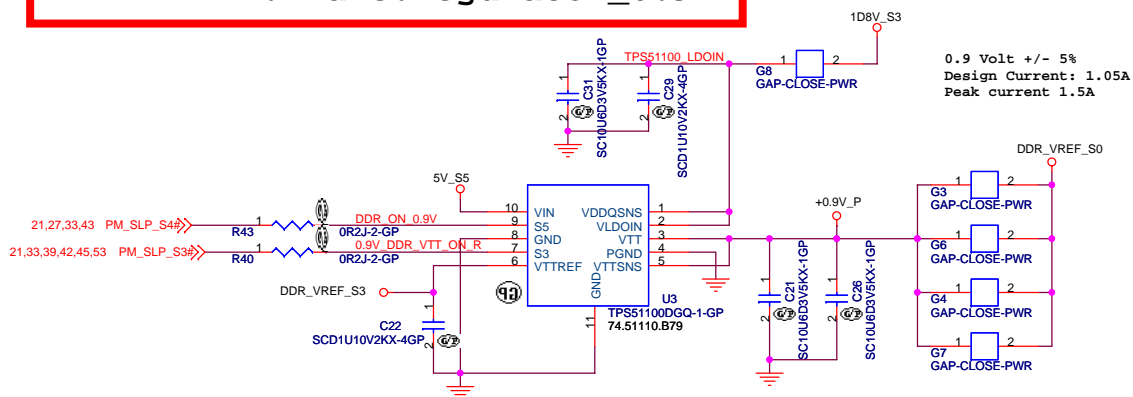
<Core Design>

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DC-DC VCCCPUCORE 1/2			
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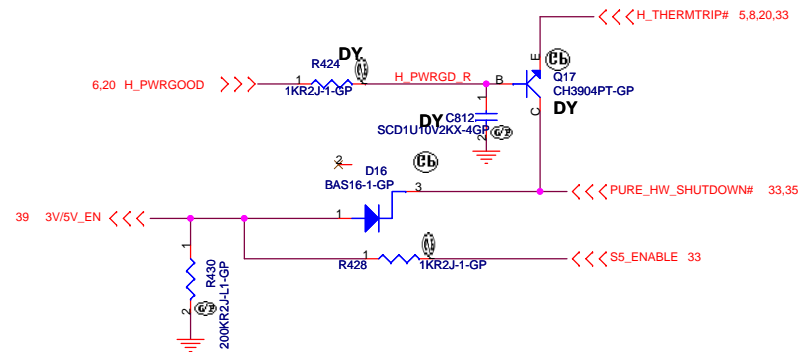
SSID = PWR.Plane.Regulator_0.9V



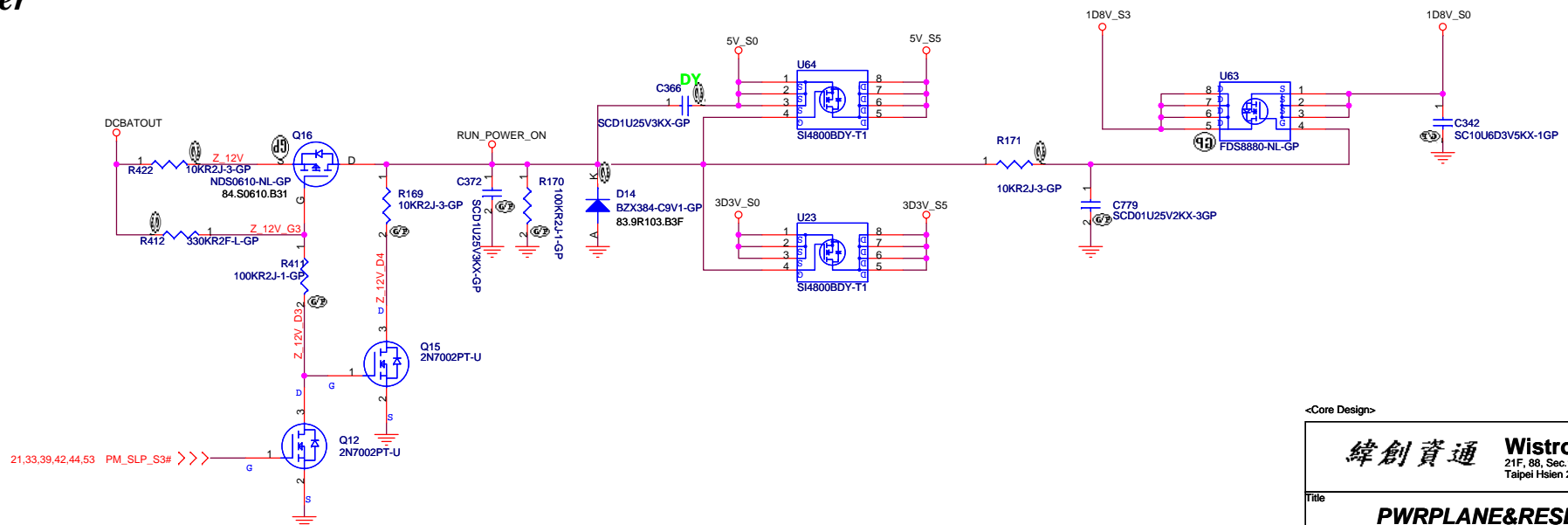
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
DC to DC 1D5V / 0D9V /1D25V		
Size	Document Number	Rev
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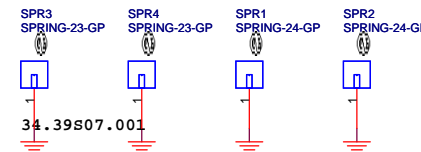
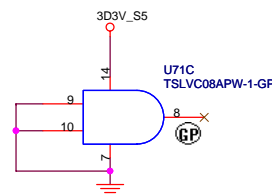
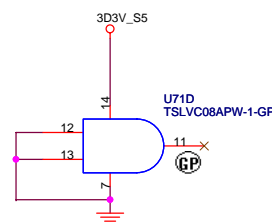
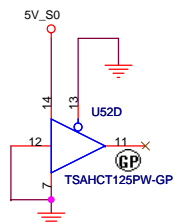
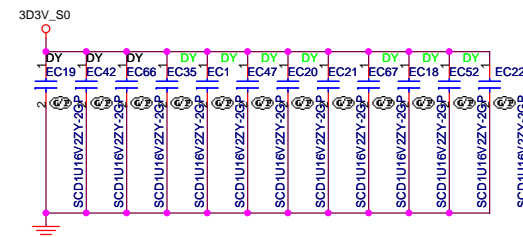
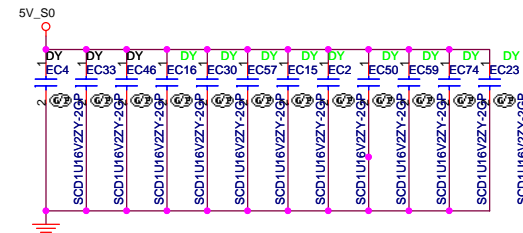
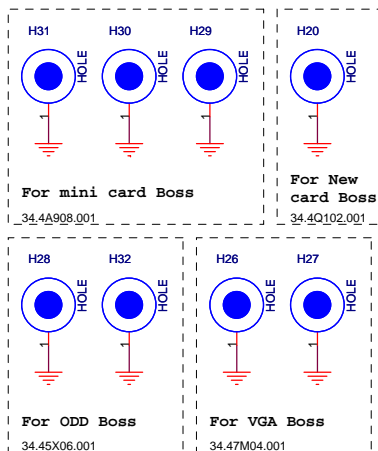
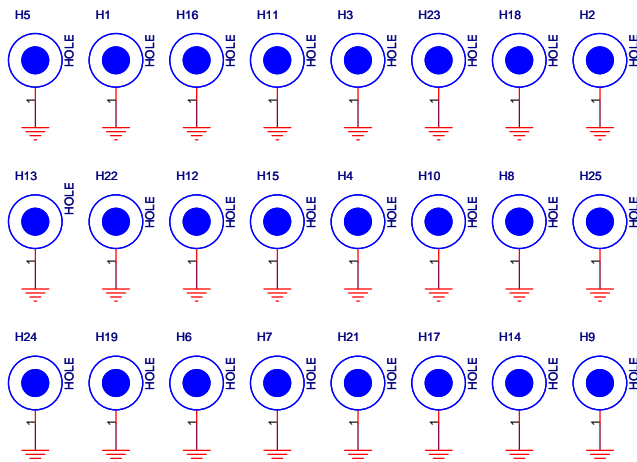
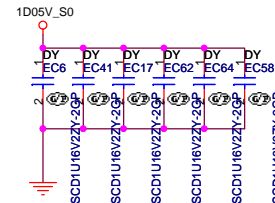
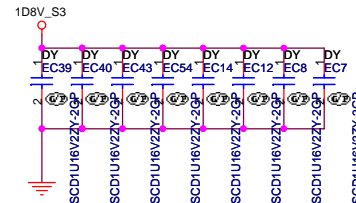
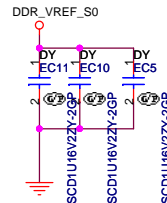
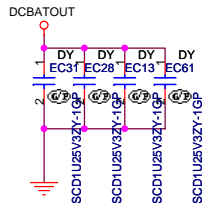
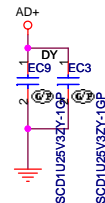
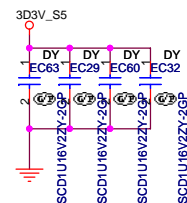
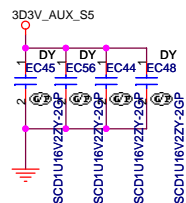
Run Power



<Core Design>

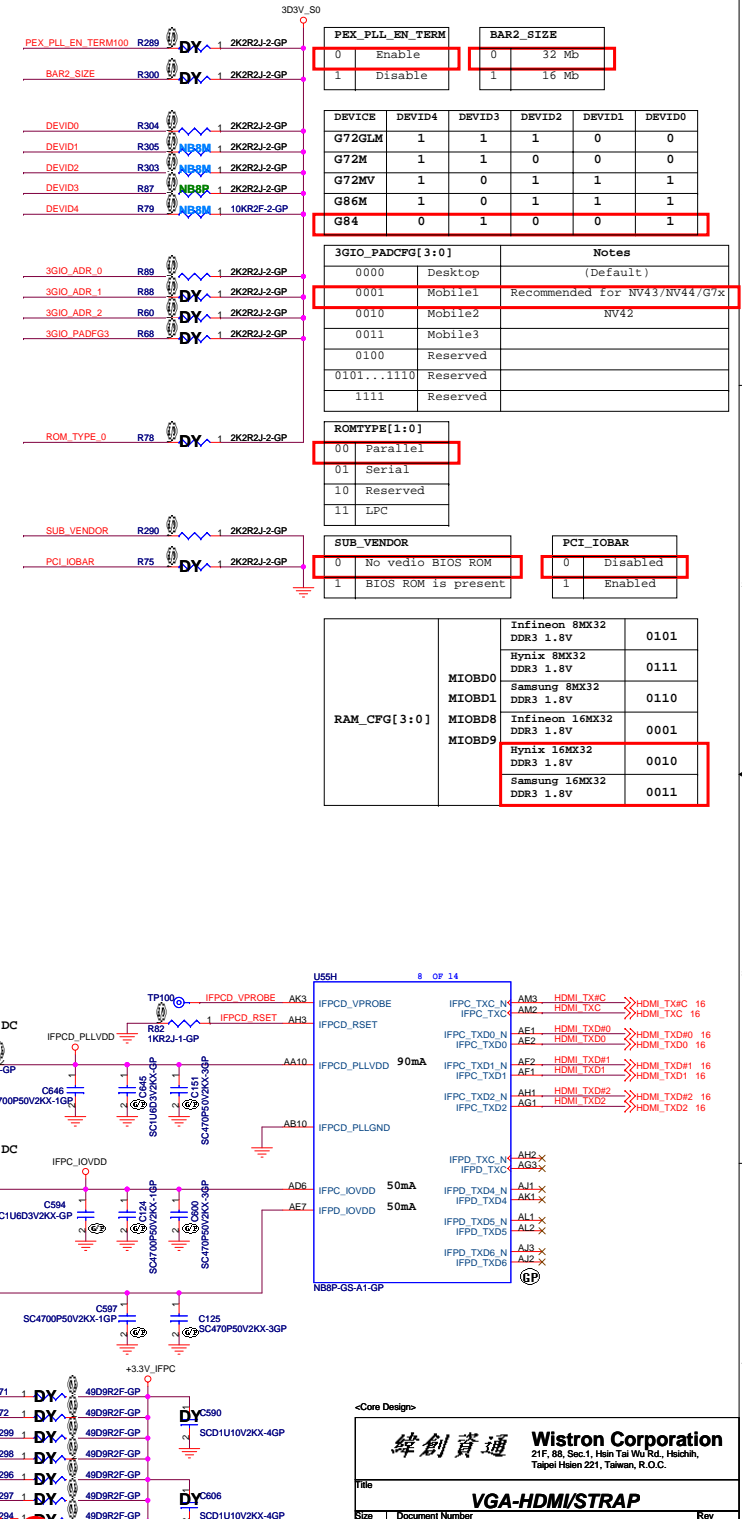
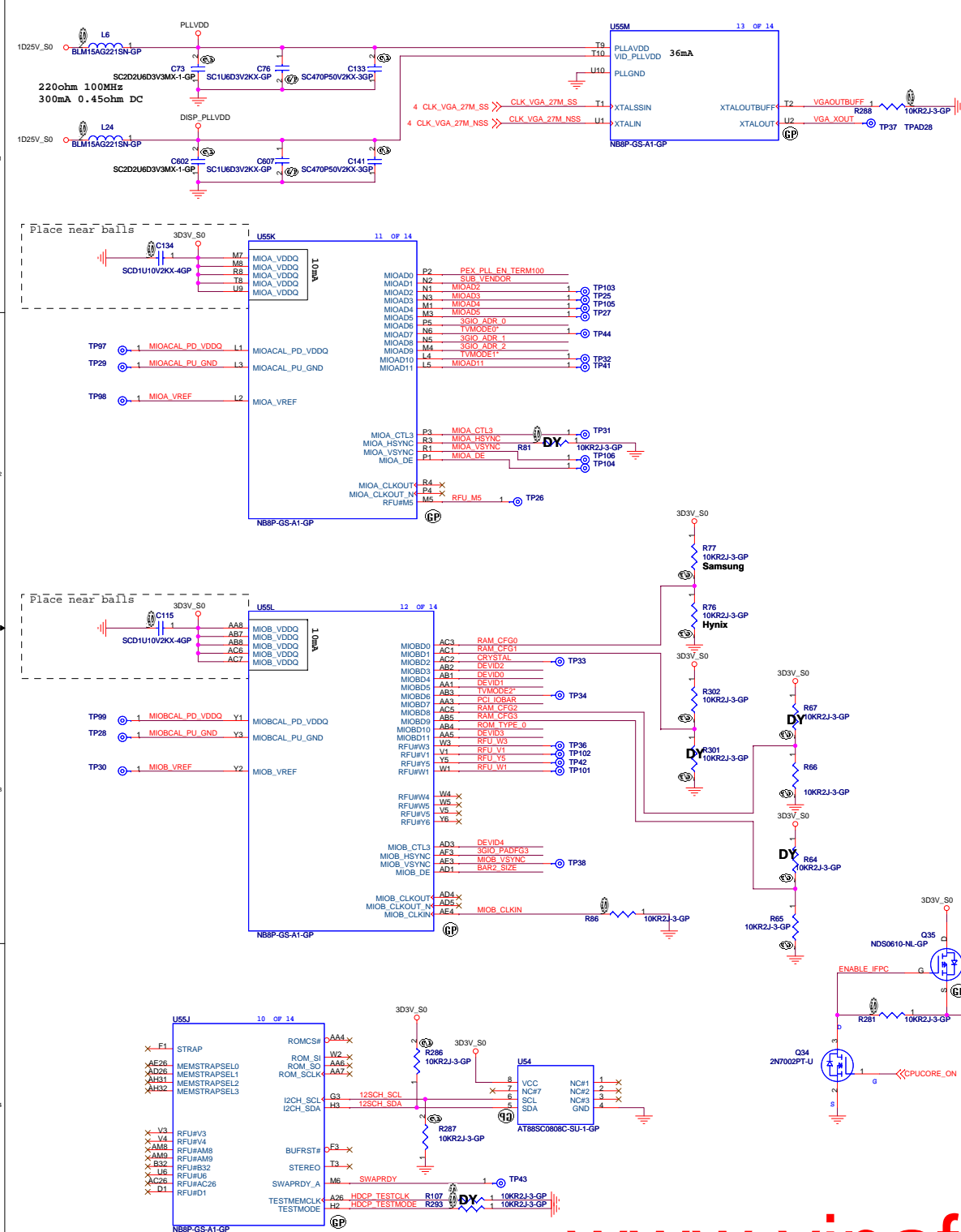
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

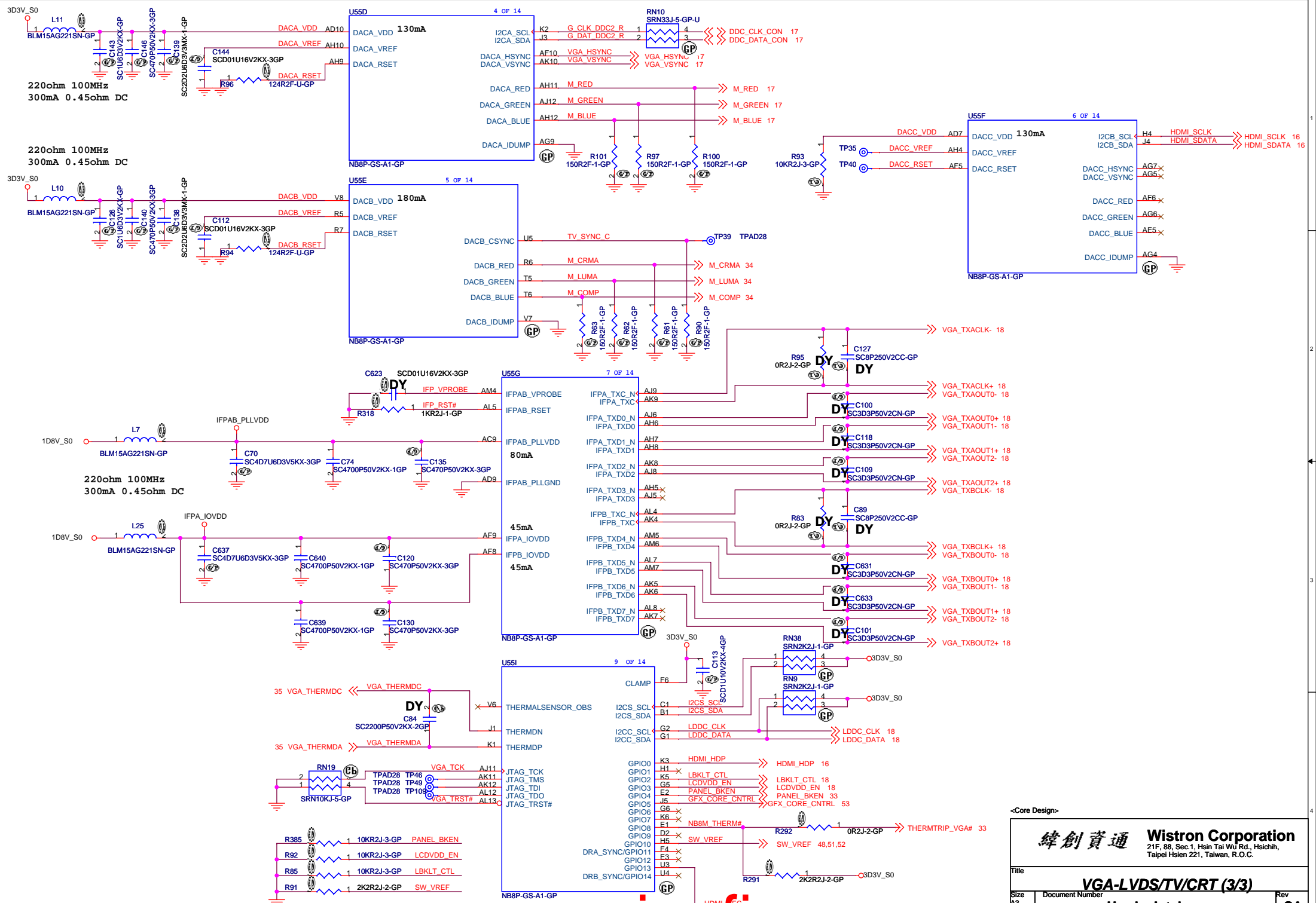
Title		PWRPLANE&RESETLOGIC	
Size A3	Document Number	Hawke-Intel	Rev SA
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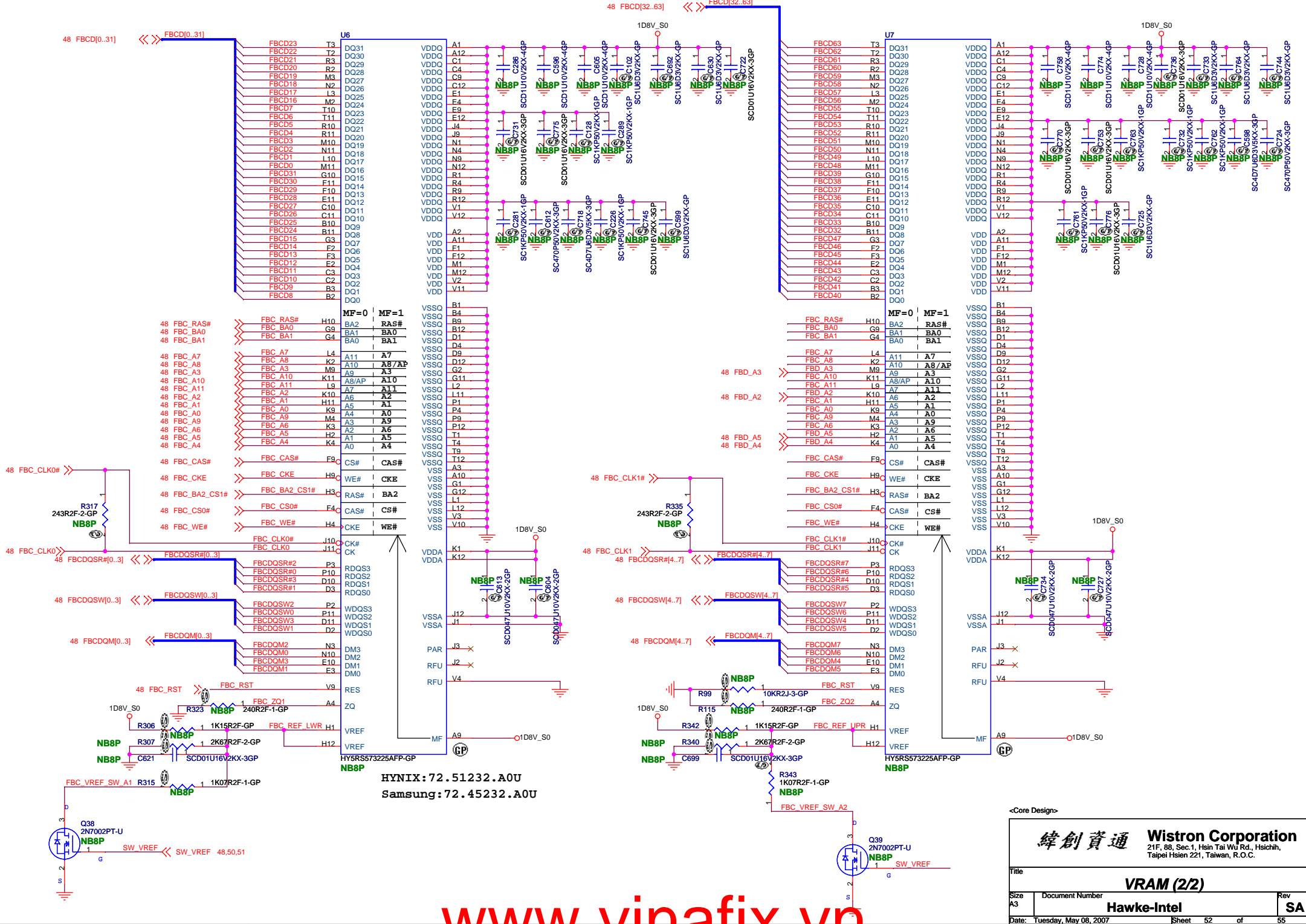
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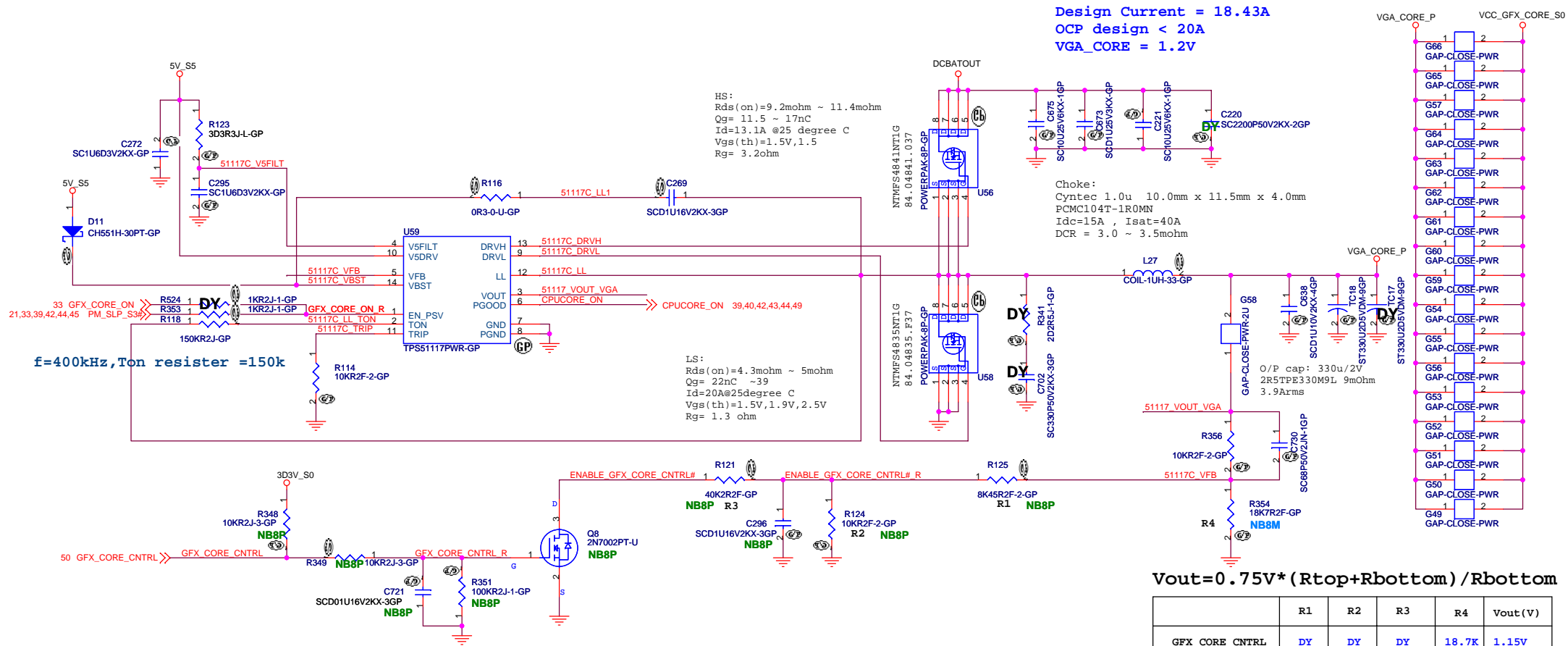
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
MISC		
Size A3	Document Number	Rev SA
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$$V_{out} = 0.75V \cdot (R_{top} + R_{bottom}) / R_{bottom}$$

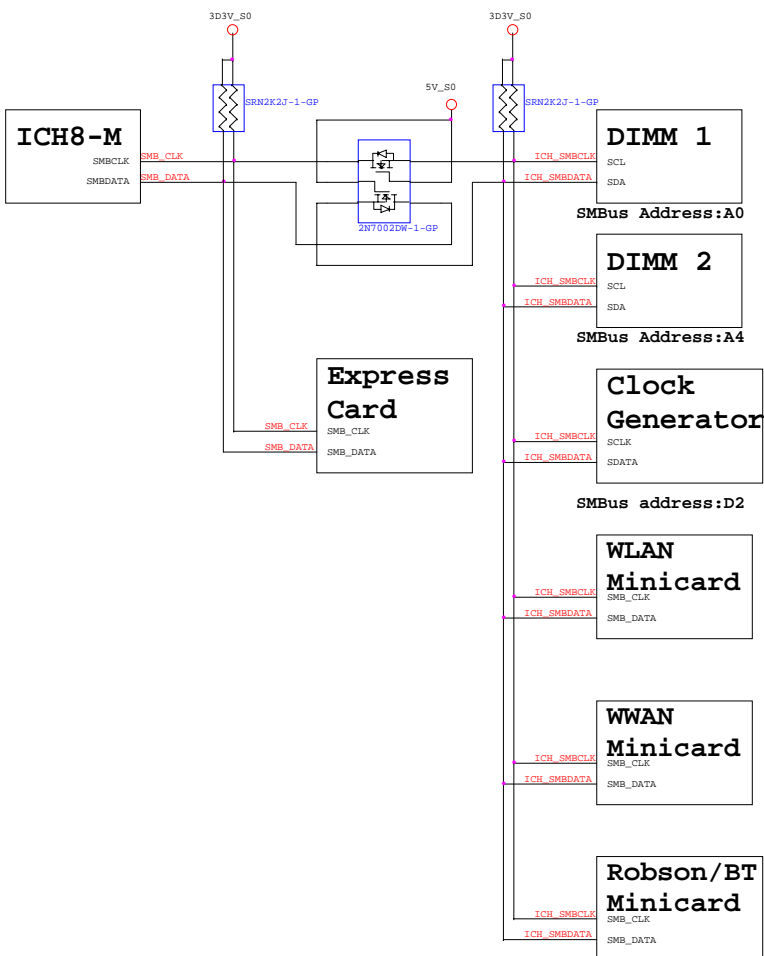
	R1	R2	R3	R4	Vout (V)
GFX_CORE_CNTRL NA	DY	DY	DY	18.7K	1.15V
GFX_CORE_CNTRL Low	8.45K	10K	40.2K to FET	DY	1.15V
GFX_CORE_CNTRL High	8.45K	10K	40.2K to GND	DY	1.2V

<Core Design>

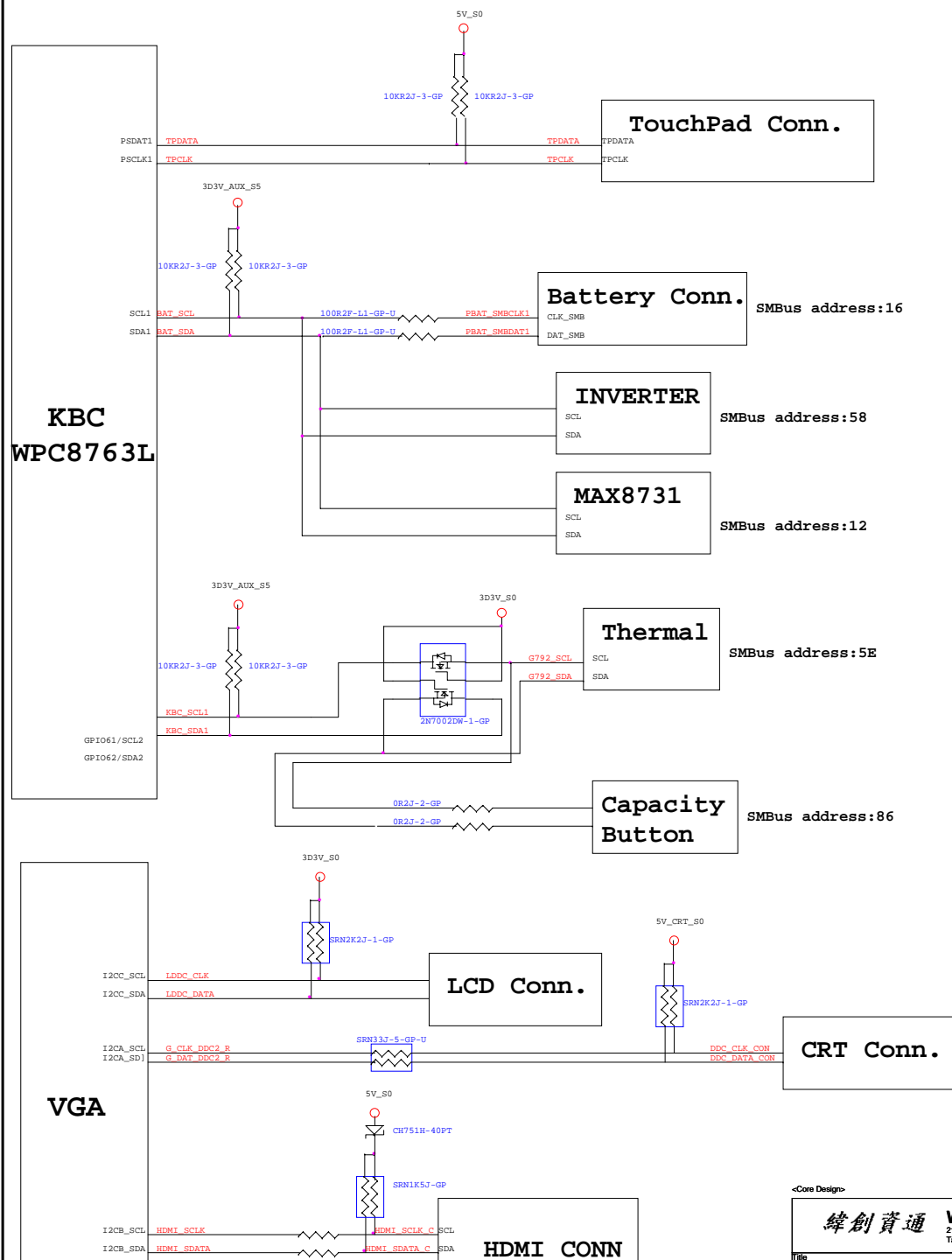
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title	DCDC VGA Core			Rev
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ICH8 SMBus Block Diagram

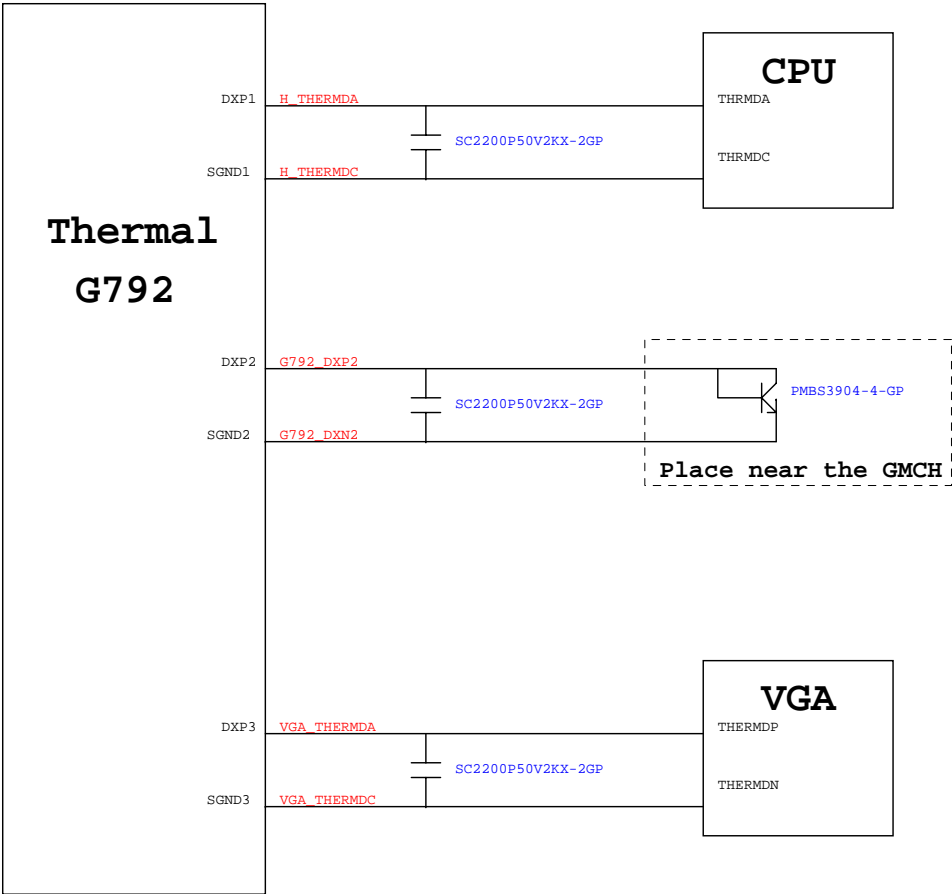


KBC SMBus Block Diagram



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Thermal Block Diagram



Audio Block Diagram

